FingerChip® Thermal Fingerprint Sweep Sensor, Hardware Based Navigation and Click Functions, Extended I/O range (1.8-3.3V)

AT77C105A Preliminary

1. Features

- **Thermal Sensitive Layer Over a 0.35 µm CMOS Array**
- **Image Zone: 0.4 ×11.6 mm**
- **Image Array: 8 × 232 = 1856 Pixels**
- **Pixel Pitch: 50 × 50 µm = 500 dpi Resolution**
- **On-chip 8-bit Analog to Digital Converter**
- **Serial Peripheral Interface (SPI) - 2 Modes:**
  - **Fast Mode at 16 Mbps Max for Imaging**
  - **Slow Mode at 200 kbps Max for Navigation and Control**
- **Die Size: 1.5 × 15 mm**
- **Operating Voltage: 2.3 to 3.6V**
- **I/O Voltage: 1.65 to 3.6V**
- **Operating Temperature Range: -40°C to 85°C**
- **Finger Sweeping Speed from 2 to 20 cm/Second**
- **Low Power: 4.5 mA (Image Acquisition), 1.5 mA (Navigation), <10 µA (Sleep Mode)**
- **Hard Protective Coating (>4 Million Sweeps)**
- **High Protection from Electrostatic Discharge**
- **Small Form Factor Packaging**
- **Comply with the European Directive for Restriction of Hazardous Substances (RoHS Directive)**

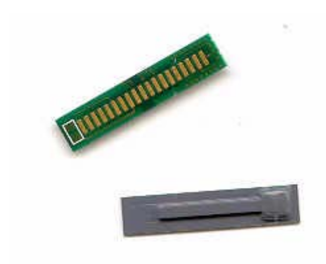
2. Description

Atmel's AT77C105A fingerprint sensor is dedicated to PDA, cellular and smartphone applications. Based on FingerChip thermal technology, the AT77C105A is a linear sensor that captures fingerprint images by sweeping the finger over the sensing area. This product embeds true hardware-based 8-way navigation and click functions as well, as enabling elimination of mechanical joystick devices.

3. Applications

- Scrolling, Menu and Item Selection for PDAs, Cellular or Smartphone Applications
- Cellular and Smartphones-based Security (Device Protection, Network and ISP Access, E-commerce)
- Personal Digital Agenda (PDA) Access
- User Authentication for Private and Confidential Data Access
- Portable Fingerprint Acquisition

Chip-on-board Package



5419C–BIOM–02/06

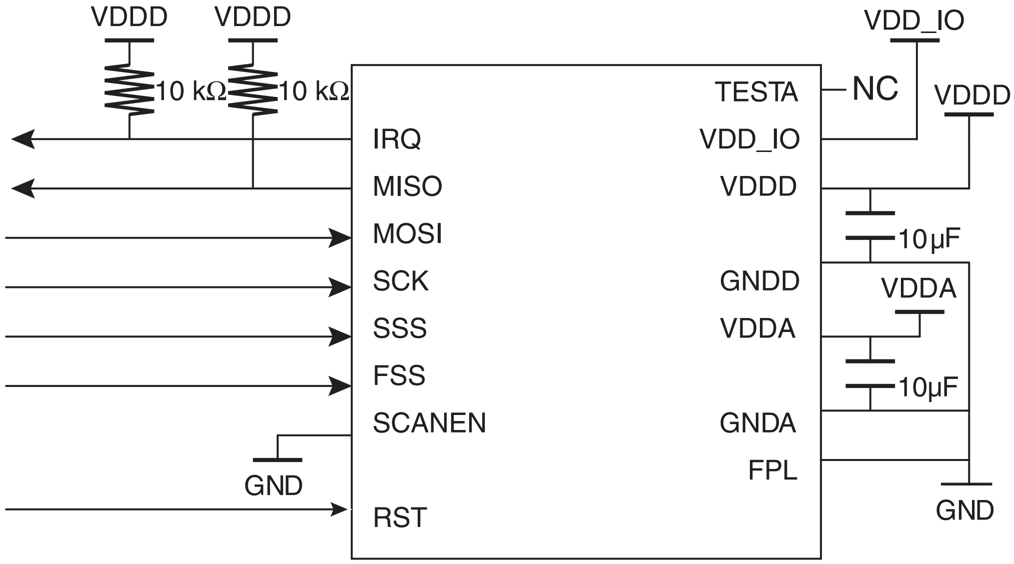
Actual size of sensor

Table 3-1. Pin Description for Chip-on-board Package: AT77C105A-CB08YV

Pin Number	Name	Type	Description
1			Not connected
2			Not connected
3			Not connected
4			Not connected
5	GNDD	G	Digital ground supply
6	GNDA	G	Analog ground supply - connect to GNDD
7	VDDD	P	Digital power supply
8	VDDA	P	Analog power supply - connect to V_{DD}
9	SCK	I	Serial Port Interface (SPI) clock
10	TESTA	IO	Reserved for the analog test, not connected
11	MOSI	I	Master-out slave-in data
12	VDD_IO	P	Input/output power supply - connect IO voltage compatibility accordingly
13	MISO	O	Master-in slave-out data
14	SCANEN	I	Reserved for the scan test in factory, must be grounded
15	SSS	I	Slow SPI slave select (active low
16	IRQ	O	Interrupt line to host (active low). Digital test pin
17	FSS	I	Fast SPI slave select (active low)
18	RST	I	Reset and sleep mode control (active high)
19	FPL	I	Front plane, must be grounded

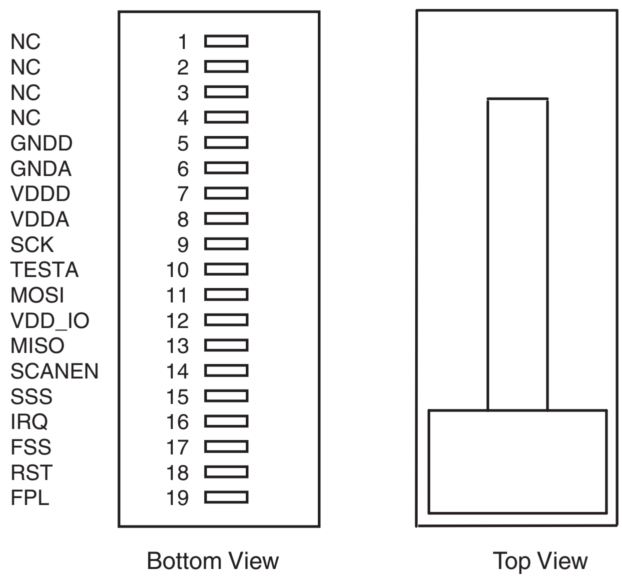
Note: The die attach is connected to pin 6 and must be grounded. The FPL pin must also be grounded.

Figure 3-1. Typical Application



The pull-up must be implemented for the master controller. The noise should be lower than 30 mV peak-to-peak on VDDA.

Table 3-2. Pin Description



The TESTA pin is only used for testing and debugging. The SCANEN pin is not used in the final application and must be connected to ground.

Warning: SSS and FSS must never be low at the same time. When both SSS and FSS equal 0, the chip switches to scan test mode. With the SPI protocol, this configuration is not possible as only one slave at a time can be selected. However, this configuration works when debugging the system.

4. Specifications

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	
Power supply voltage	VDDD, VDDA		-0.5 to 4.6V	Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Front plane	FPL		GND to V_{DD} +0.5V	
Digital input	SSS, FSS, SCK, MOSI		GND to V_{DD} +0.5V	
Input/output pads power supply	VDD_IO		GND to V_{DD} +0.5V	
Storage temperature	T_{stg}		-50 to +95°C	
Lead temperature (soldering 10 seconds)	T_{leads}	Do not solder	Forbidden	

Table 4-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Positive supply voltage	V_{DD}	2.5 ±5% 3.3 ±10%	2.3	2.5 3.3	3.6	V
I/O pads power supply	V_{DD_IO}	2.8 ±8%	1.65	1.8	VDD	V
Front plane	FPL	Must be grounded	GND			V
Digital input voltage			CMOS levels			V
Digital output voltage			CMOS levels			V
Digital load	C_L			20	50	pF
Operating temperature range	T_{amb}	Industrial “V” grade	-40 to +85			°C
Maximum current on VDDA	IVDDA		0	-	60	mA

Table 4-3. Resistance

Parameter	Min Value	Standard Method
ESD		
On die surface (zap gun) air discharge	±16 kV	NF EN 6100-4-2
Mechanical Abrasion		
Number of cycles without lubricant Multiply by a factor of 20 for correlation with a real finger	200 000	MIL E 12397B
Chemical Resistance		
Cleaning agent, acid, grease, alcohol, diluted acetone	4 hours	Internal method

Note: TBC = To be confirmed

Table 4-4. Explanation of Test Levels

Level	Description
I	100% production tested at +25°C
II	100% production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample)
III	Sample tested only
IV	Parameter is guaranteed by design and/or characterization testing
V	Parameter is a typical value only
VI	100% production tested at temperature extremes
D	100% probe tested on wafer at T_{amb} = +25°C

Table 4-5. Specifications

Parameter	Symbol	Test Level	Min[(1)]	Typ	Max[(1)]	Unit
Resolution		IV	50			Micron
Size		IV	8 × 232			Pixel
Yield: number of bad pixels		I			5	Bad pixels

5. Power Consumption and DC Characteristics

The following characteristics are applicable to the operating temperature -40°C ≤ T ≤ +85°C.
Typical conditions are: power supply = 3.3V; T_{amb} = 25°C; F_{SCK} = 12 MHz (1600 slices per second); duty cycle = 50% C_{LOAD} 120 pF on digital outputs unless otherwise specified.

Table 5-1. Power Requirements

Name	Parameter	Conditions	Test Level	Min[(1)]	Typ	Max[(1)]	Unit-
V_{DD}	Positive supply voltage		I	2.3	2.5/3.3	3.6	V
I_{DD}	Current on V_{DD} in acquisition mode		I	3	4.5	6	mA
I_{DDNAV}	Current on V_{DD} in navigation mode		I	1	1.5	2	mA
I_{DDCLI}	Current on V_{DD} in click mode		I	0.2	0.3	0.5	mA
I_{DDSLP}	Current on V_{DD} in sleep mode		I			10	µA
I_{DDSTB}	Current on V_{DD} in stand-by mode		I	Refer to ”Power Management” on page 29			

Note: 1. Min and max values are to be confirmed.

5.1 VDD_IO = 1.8V

Table 5-2. Digital Inputs

Logic Compatibility		**CMOS**					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
I_{IL}	Low level input current without pull-up device(1)	$V_I = 0V$	I			1	µA
I_{IH}	High level input current without pull-down device(1)	$V_I = V_{DD\_IO}$	I			1	µA
I_{IOZ}	Tri-state output leakage without pull-up/down device(1)	$V_I = 0V$ or V_{DD_IO}	IV			1	µA
V_{IL}	Low level input voltage(1)		I			0.4 V_{DD_IO}(1)	V
V_{IH}	High level input voltage(1)		I	0.6 V_{DD}(1)			V
V_{HYST}	Schmitt trigger hysteresis(1)		IV	0.15 V_{DD_IO}		0.3 V_{DD_IO}	V

Table 5-3. Digital Outputs

Logic Compatibility		**CMOS**					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Low level output voltage	$I_{OL} = 4$ mA $V_{DD} = 1.8V \pm 8\%$	I			0.15 V_{DD_IO} (1)	V
V_{OH}	High level output voltage	$I_{OH} = -4$ mA $V_{DD} = 3.3V \pm 10\%$	I	0.85 V_{DD}			V

Note: 1. A minimum noise margin of 0.05 V_{DD} should be taken for Schmitt trigger input threshold switching levels compared to V_{IL} and V_{IH} values.

5.2 VDD_IO = 2.3V to 3.6V

Table 5-4. Digital Inputs

Logic Compatibility		CMOS					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
I_{IL}	Low level input current without pull-up device(1)	$V_I = 0V$	I			1	µA
I_{IH}	High level input current without pull-down device(1)	$V_I = V_{DD\_IO}$	I			1	µA
I_{IOZ}	Tri-state output leakage without pull-up/down device(1)	$V_I = 0V$ or V_{DD_IO}	IV			1	µA
V_{IL}	Low level input voltage(1)		I			0.5 V_{DD_IO}(1)	V
V_{IH}	High level input voltage(1)		I	0.6 V_{DD_IO}(1)			V
V_{HYST}	Schmitt trigger hysteresis(1)		IV	0.06 V_{DD_IO}		0.09 V_{DD_IO}	V

Table 5-5. Digital Outputs

Logic Compatibility		CMOS					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Low level output voltage	$I_{OL} = 4$ mA $V_{DD\_IO} = 2.3V$ to 3.6V	I			0.10 V_{DD_IO}(1)	V
V_{OH}	High level output voltage	$I_{OH} = -4$ mA $V_{DD\_IO} = 2.3V$ to 3.6V	I	0.90 V_{DD}			V

5.3 Input/Output Voltage Level Compatibility

The I/O voltage level compatibility is set by the power voltage driven on the VDD_IO pad. For 1.8V level compatibility, connect VDD_IO to a 1.8V power supply.

6. Switching Performances

The following characteristics are applicable to the operating temperature -40°C ≤ T ≤ +85°C.
Typical conditions are: nominal value; T_{amb} = 25°C; F_{SCK} = 12 MHz; duty cycle = 50%; C_{LOAD} 120 pF in digital output unless specified otherwise.

Table 6-1. Timings

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Clock frequency acquisition mode	F_{ACQ}	IV	8		16	MHz
Clock frequency navigation mode and chip control	F_{CTRL}	I	-		0.2	MHz
Duty cycle (clock SCK)	DC	IV	20	50	80	%
Reset setup time	T_{RSTSU}	I	½ T_{SCK}[(1)]			ns
Slave select setup time	T_{SSSU}	I	½ T_{SCK}[(1)]			ns
Slave select hold time	T_{SSHD}	I	½ T_{SCK}[(1)]			ns

Note: 1. $T_{SCK} = 1/F_{CTRL}$ (clock period)

Table 6-2. 3.3V ±10% Power Supply

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Data in setup time	T_{SU}	IV		3		ns
Data in hold time	T_H	IV		1		ns
Data out valid	T_V	I			30	ns
Data out disable time from SS high	T_{DIS}	IV		3.8		ns
IRQ hold time	T_{IRQ}	IV			3	µs

Note: All power supplies = +3.3V

Table 6-3. 2.5V ±5% Power Supply

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Data in setup time	T_{SU}	IV		3		ns
Data in hold time	T_H	IV		1		ns
Data out valid	T_V	I			30	ns
Data out disable time from SS high	T_{DIS}	IV		3.8		ns
IRQ hold time	T_{IRQ}	IV			3	µs

Note: All power supplies = +2.5V

Table 6-4. 1.8V ±5% Power Supply

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Data in setup time	T_{SU}					ns
Data in hold time	T_H					ns
Data out valid	T_V					ns
Data out disable time from SS high	T_{DIS}					ns
IRQ hold time	T_{IRQ}					μs

7. Timing Diagrams: Slow and Fast SPI Interface

Figure 7-1. Read Timing Fast SPI Slave Mode

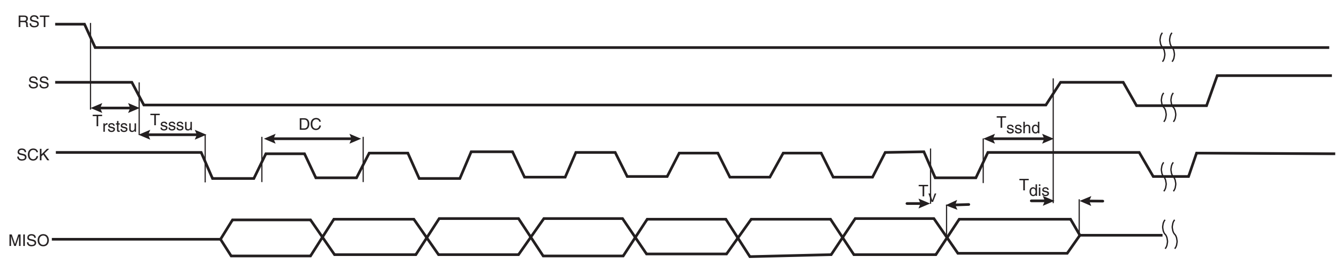


Figure 7-2. Read/Write Timing Slow SPI Slave Mode

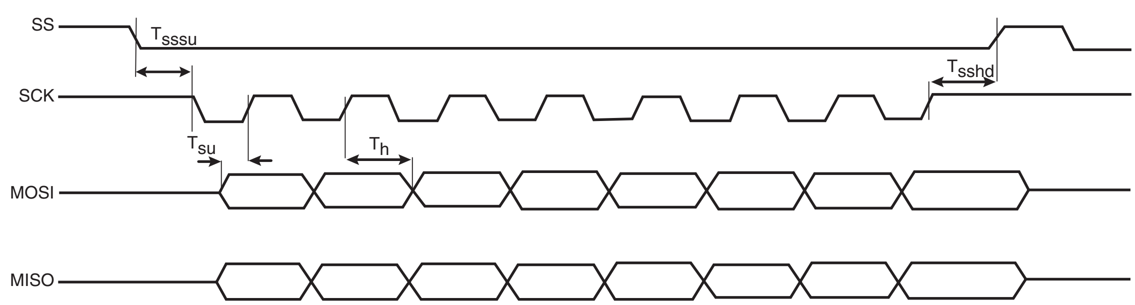


Figure 7-3. Read Status Register to Release IRQ

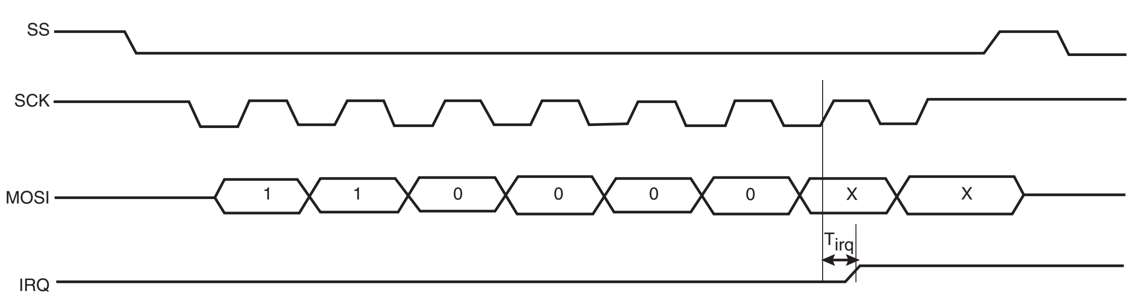
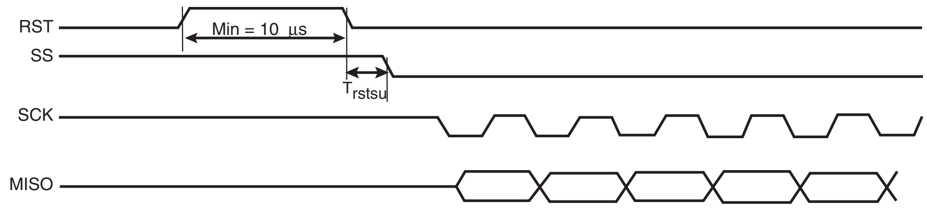


Figure 7-4. Chip Initialization



8. Functional Description

The AT77C105A is a fingerprint sensor based on FingerChip technology. It is controlled by an SPI serial interface through which output data is also transferred (a slow SPI for the pointing function and a fast one for acquisition). Six modes are implemented:

– **Sleep Mode:** A very low consumption mode controlled by the reset pin RST. In this mode, the internal clocks are disabled and the registers are initialized.

– **Stand-by Mode:** Also a low consumption mode that waits for an action from the host. The slow serial port interface (SSPI) and control blocks are activated. In this mode the oscillator can remain active.

– **Click Mode:** Waits for a finger on the sensor. The SSPI and control blocks are activated. The local oscillator, the click array and the click block are all activated.

– **Navigation Mode:** Calculates the finger's x and y movements across the sensor. The SSPI and control blocks are still activated. The local oscillator, the navigation array and the navigation block are also activated.

– **Acquisition Mode:** Slices are sent to the host for finger reconstruction and identification. The SSPI and control blocks are still activated. The fast serial port interface block (FSPI) and the acquisition array are activated, as well as the local oscillator when watchdog is required.

– **Test:** This mode is reserved for factory testing.

In the final application, three main modes are used:

– **Stand-by:** Low consumption mode

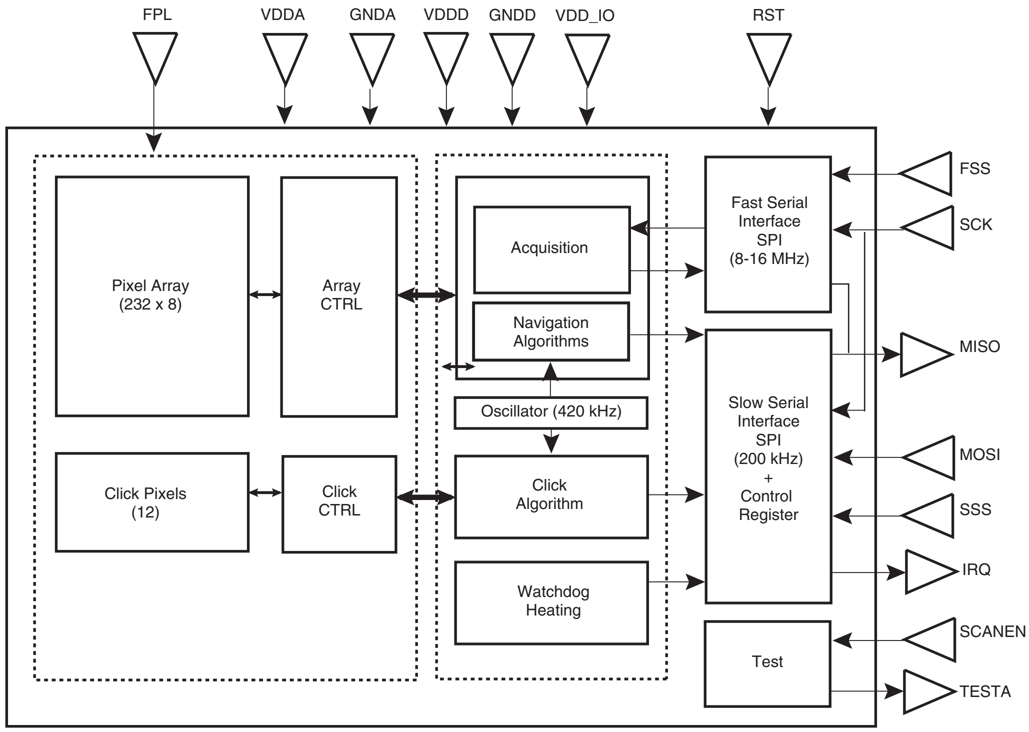
– **Pointing:** Equivalent to click and navigation modes

– **Acquisition:** Fingerprint image capture

Note: The term"host" describes the processor (controller, DSP...) linked to the sensor. It is the master. In the description of n-bit registers (see "Function Registers" on page 11), the term "b0" describes the Least Significant Bit (LSB). The term "b(n-1)" describes the Most Significant Bit (MSB). Binary data is written as 0b_ and hexadecimal data as 0x_.

9. Sensor and Block Diagram

Figure 9-1. Functional Block Diagram



The circuit is divided into the following main sections:

- An array or frame of 8 × 232 pixels + 1 dummy column
- An analog to digital converter
- An on-chip oscillator
- Control and status registers
- Navigation and click units
- Slow and fast serial interfaces

10. Function Registers

Table 10-1. Registers

Register	Address (b3 down to b0)	Read/Write
STATUS	0000	Read
MODECTRL	0001	Read/Write
ENCTRL	0010	Read/Write
HEATCTRL	0011	Read/Write
NAVCTRL	0100	Read/Write
CLICKCTRL	0101	Read/Write

Table 10-1. Registers (Continued)

Register	Address (b3 down to b0)	Read/Write
MOVCTRL	0110	Read/Write
	0111	Reserved
NAVIGATION[(1)]	1000	Read
NAVIGATION[(1)]	1001	Reserved
NAVIGATION[(1)]	1010	Reserved
PIXELCLICK	1011	Reserved
PIXELCLICK	1100	Reserved
PIXELCLICK	1101	Reserved
	1110	Reserved

Note: 1. Navigation requires 3 registers. The reading of the first register (0b1000) enables the reading of all 3 registers.

10.1 Status Register

Register Name: Status (8 bits)

Access Type: Read Only

Function: State of AT77C105A

b7	b6	b5	b4	b3	b2	b1	b0
CLICK	MOV	TRANSIT	SLICE	READERR	–	–	–
0	0	0	0	0	0	0	0

- **CLICK:** Click detection
  0: default
  1: click detected
- **MOV:** Movement detection
  0: default
  1: X or Y movement detected
- TRANSIT: Not used, for testing only
- SLICE: Not used, for testing only
- **READERR:** Read error detection
  0: default, no error
  1: read error detected

Note: To clear the interrupts, the status register is initialized after each reading from the host.

10.2 Modectrl Register

Register Name: Modectrl (7 bits)

Access Type: Read/Write

Function: Mode control

b6	b5	b4	b3	b2	b1	b0
MODE (MSB)	MODE	MODE	MODE (LSB)	ANALOGRST	–	–
0	0	0	0	1	0	0

- **MODE:** Select operating mode
  0000: standby
  0001: test (reserved for factory use)
  0010: click
  0100: navigation
  1000: acquisition

Certain changes can be made. For example, MODE can be set to 0b0110 to activate click and navigation.

- **ANALOGRST:** Reset local oscillator
  0: oscillator in active mode
  1: oscillator in power-down mode

Notes:
1. Click or navigation modes cannot be used when the local oscillator is switched off..
2. To return to standby mode and stop the oscillator (to save on power consumption), two Modectrl register accesses are necessary: the first one to select standby mode and the second to switch off the oscillator.
3. The read-only registers cannot be read when the oscillator is turned off.
4. To shift between navigation and acquisition modes, you must be in standby mode (Modectrl = 0b00001).

If modes such as "acquisition and click" or "acquisition and navigation" are programmed together, they will be ignored by the system.

Programmed Mode	Register Value
11xx	01xx
1x1x	0x1x

With x = 0 or 1.

10.3 Enctrl Register

Register Name: Enctrl (7 bits)

Access Type: Read/Write

Function: Interrupts control

b6	b5	b4	b3	b2	b1	b0
CLICKEN	MOVEN	TRANSITEN	SLICEN	READERREN	–	–
0	0	0	0	0	0	0

- **CLICKEN:** Click interrupts enable
  0: default
  1: click IRQ enabled

IRQ is generated when a click is detected.

- **MOVEN:** Movement interrupts enable
  0: default
  1: movement IRQ enabled

IRQ is generated when an X or Y movement is detected.

- **TRANSITEN:** Not used, for testing only
- **SLICEN:** Not used, for testing only
- **READERREN:** Read error interrupts enable
  0: default
  1: read error IRQ enabled

IRQ is generated when a read error is detected.

Note: The interrupt is cleared after the status register is read.

10.4 Heatctrl Register

Register Name: Heatctrl (7 bits)

Access Type: Read/Write

Function: Heating control

b6	b5	b4	b3	b2	b1	b0
HEAT	WDOGEN	HEATV (MSB)	HEATV(LSB)	–	–	–
0	0	0	0	0	0	0

- **HEAT:** Sensor heating
  0: default, no heating
  1: heating
  The default value is recommended to optimize power consumption.
- **WDOGEN:** Watchdog enable
  0: default
  1: watchdog enabled
  Watchdog automatically stops heating of the sensor after a time-out.
- **HEATV (2 bits):** Heating power value
  00: 50 mW
  01: 100 mW
  10: reserved
  11: reserved

V_{DD} is between 2.5 and 3.6V.

Notes: 1. Heating can only be used in the acquisition mode (it is not allowed in navigation or click modes).
2. The oscillator has to be activated when the watchdog is required and must not be stopped while the watchdog remains active.

10.5 Navctrl Register

Register Name: Navctrl (7 bits)

Access Type: Read/Write

Function: Navigation control

b6	b5	b4	b3	b2	b1	b0
NAVFREQ (MSB)	NAVFREQ (LSB)	NAVV (MSB)	NAVV (LSB)	CLICKV (MSB)	CLICKV (LSB)	reserved
1	0	0	0	0	0	0

- **NAVFREQ:** Navigation frequency
  00: 5.8 kHz
  01: 2.9 kHz (default value)
  10: 1.9 kHz
  11: 1.5 kHz

A faster frequency enables faster finger movement detection. A lower frequency enhances sensitivity. Refer to Notes 1 and 2 on page 15.

- **NAVV:** Navigation pixels threshold
  00: lower threshold
  01:
  10:
  11: higher threshold

Sets the minimum analog value detected as a high level (‘1’). Refer to Note 1 on page 15.

- **CLICKV:** Click pixels threshold
  00: lower threshold
  01:
  10:
  11: higher threshold

Sets the minimum analog value detected as a high level (‘1’) and the maximum analog value detected as a low level (‘0’). See Note 3 on page 15.

Notes: 1. Navfreq and Navv registers should not be changed once the navigation mode is selected. Finger sensitivity refers to the minimum level of information required from a finger. The sensitivity is linked to the integration time; a longer integration time enables better sensitivity but does not tolerate fast movement.
2. The navigation frequency is the frequency needed for the reading of one new navigation frame.
3. The Clickv register should not be changed once the click mode is selected.

10.6 Clickctrl Register

Register Name: Clickctrl (7 bits)

Access Type: Read/Write

Function: Click control

b6	b5	b4	b3	b2	b1	b0
CLICKFREQ (MSB)	CLICKFREQ (LSB)	CLICKDET (MSB)	CLICKDET (LSB)	CLICKCPT (MSB)	CLICKCPT	CLICKCPT (LSB)
0	1	0	1	1	0	1

- **CLICKFREQ:** Click pixels reading frequency
  00: 180 Hz
  01: 90 Hz (default value)
  10: 60 Hz
  11: 45 Hz

Faster frequency enables faster finger click detection. Lower frequency enables higher sensitivity.

- **CLICKDET:** Threshold for selecting the black/white color of a slice
  00: more than 7 black/white pixels and less than 5 white/black pixels
  01: more than 8 black/white pixels and less than 4 white/black pixels
  10: more than 9 black/white pixels and less than 3 white/black pixels
  11: more than 10 black/white pixels and less than 2 white/black pixels

- **CLICKCPT:** Click detection counter (maximum number of slices read between two transitions)
  000: 5
  001: 7
  010: 10
  011: 12
  100: 16
  101: 20
  110: 25
  111: 31

Two transitions are interpreted as a click if the number of slices between them is less than CLICKCPT. This is used to differentiate a touch-down/touch-up from a real click. A click is equivalent to two close touch-down/touch-up transitions.

This register adjusts the “time out” for considering the two transitions as a click.

Note: Clickfreq and Clickcpt registers should not be changed once the click mode is selected.

10.7 Movectrl Register

Register Name: Movctrl (7 bits)

Access Type: Read/Write

Function: In stream mode, during navigation calculation, the AT77C105A must interrupt the host when a maximum absolute X or Y movement is detected (second and third navigation registers). The MOVECTRL register enables you to control this value. This value can be set as the minimum finger movement value at which the pointing device makes a displacement.

b6	b5	b4	b3	b2	b1	b0
(MSB)	–	–	–	–	–	(LSB)
0	0	0	0	0	0	0

- MOVCTRL: Generates an interrupt when the second or third navigation register (X or Y absolute movement) is greater than the value programmed in the Movectrl register
  0b0000000
  0b0000001
  0b0000010
  ...
  0b1111111

For example, when MOVCTRL = 0b0001001, an interruption to the host is generated when the absolute X movement register (second navigation register) or absolute Y movement register (third navigation register) is greater than 0b00010010.

Note: The Movctrl register should not be changed once the navigation mode is selected.

10.8 Navigation Register

Register Name: Navigation (3 x 8 bits)

Access Type: Read Only (these three registers cannot be read individually. The reading command of the first navigation register [address 0b1000] returns the value of the three registers).

Function: The format of the navigation registers is similar to the PS/2 protocol. Three registers are used to codemovements and clicks. The navigation registers are initialized after each reading. The registers only represent actions (movement, click, transition...) that have occurred since the last data packet sent to thehost.

10.8.1 General Register

b7	b6	b5	b4	b3	b2	b1	b0
YOVR	XOVR	YSIGN	XSIGN	1	TRANS	CLICK	FINGER
0	0	0	0	1	0	0	0

- **YOVR:** Y overflow
  0: default
  1: Y movement overflow

High (‘1’) when the Y movement counter is overflowed.

- **XOVR:** X overflow
  0: default
  1: X movement overflow

High (‘1’) when the X movement counter is overflowed.

- **YSIGN:** Y sign bit
  0: default, positive Y movement
  1: negative Y movement

High (‘1’) when the Y movement is negative. Low when the Y movement is positive.

- **XSIGN:** X sign bit
  0: default, positive X movement
  1: negative X movement

High (‘1’) when the X movement is negative. Low when the X movement is positive.

- **TRANS:** Not used, for test purposes only.
- **CLICK: Click**
  0: default
  1: click detected

This function is not in the PS/2 protocol.

- **FINGER:** Not used, for test purposes only.

Note: In the PS/2 protocol, bits b2 and b1 are used to code the middle and right buttons respectively, and b3 is set to high.

10.8.2 Absolute X Movement Register (0 to 255 Pixels)

b7	b6	b5	b4	b3	b2	b1	b0
XMOV (MSB)	–	–	–	–	–	–	XMOV (LSB)
0	0	0	0	0	0	0	0

10.8.3 Absolute Y Movement Register (0 to 255 Pixels)

b7	b6	b5	b4	b3	b2	b1	b0
YMOV (MSB)	–	–	–	–	–	–	YMOV (LSB)
0	0	0	0	0	0	0	0

Note: When a click is detected, the information is placed in the b7 bit of the status register and in the b1 bit of the general navigation register. The reading of the status register initializes the b7 bit but does not initialize the b1 bit of the general navigation register. The host must carefully correlate the two bits.

11. SPI Interface General Description

Two communication busses are implemented in the device:

- The control interface, a slow bus that controls and reads the internal registers (status, navigation, control...).
- The pixels' acquisition interface, a fast bus that enables full pixel acquisition by the host.

A synchronous Serial Port Interface (SPI) has been adopted for the two communication busses.

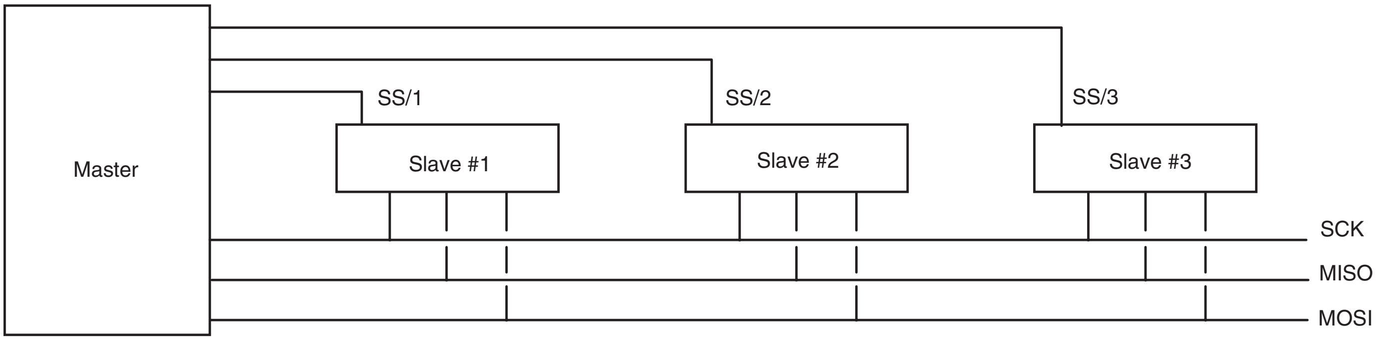
The SPI protocol is a slave/master fullduplex synchronous serial communication. This protocol uses three communication signals:

- SCK (Serial Clock): the communication clock
- MOSI (Master Out Slave In): the data line from the master to the slave
- MISO (Master In Slave Out): the data line from the slave to the master

The slaves are selected by an input pin SS/ (Slave Select). A master can communicate with several slaves.

The word length of the transferred data is fixed to 8 bits. The Most Significant Bit (MSB) is sent first. For each 8-bit transfer, 8 bits are sent from the master to the slave and 8 bits transferred from the slave to the master. Transfers are still synchronized with the communication clock (SCK). Only the host can initialize transfers. To send data, the slave must wait for an access from the master. When there is no transfer, a clock is not generated.

Figure 11-1. One Master with Several Slaves



When a master is connected with several slaves, the signals SCK, MISO and MOSI are interconnected. Each slave SS is driven separately. Only one slave can be selected, the others have their MISO tri-stated and ignore MOSI data.

The SS/ signal falls a half-period before the first clock edge, and rises a half-period after the last clock edge.

11.1 Clock Phase and Polarity

During phase zero of the operation, the output data changes on the clock's falling edge and the input data is shifted in on the clock's rising edge. In phase one of the operation, the output data changes on the clock's rising edge and is shifted in on the clock's falling edge.

Polarity configures the clock's idle level, which is high ("1") during polarity one of the operation and low ("0") during polarity zero of the operation.

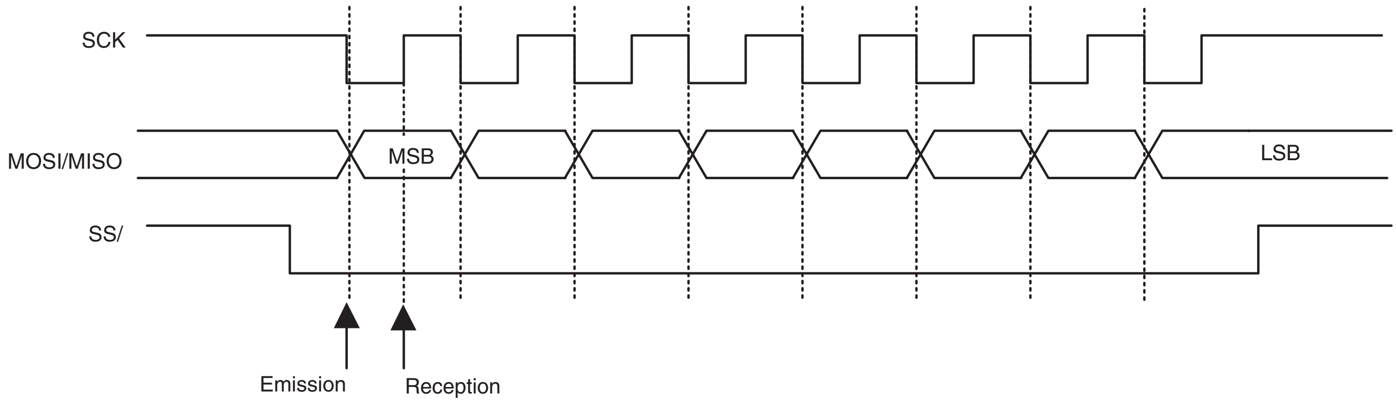
11.2 AT77C105A and the SPI

The AT77C105A is always the slave and the host always the master. The host drives the SCK clock. Both the AT77C105A and the host transmit data with the MISO signal. The word length of the transferred data is fixed to 8 bits. The Most Significant Bit (MSB) is sent first.

The AT77C105A supports only one phase and polarity configuration:

- The clock's idle level set to high (polarity 1)
- The output data changed on the clock's falling edge, and input data shifted in on the clock's rising edge (phase 0).

Figure 11-2. SPI Waveform (Phase = 0, Polarity = 1)



Note: During initialization of the SCK wire (power-on or reset), SS/ has to be inactive (“1“).

11.2.1 Recommendations

The SSS or FSS falling edge should be half a clock cycle *before* the first SCK falling edge and the SSS or FSS rising edge should be half a clock cycle *after* the last SCK rising edge.

11.3 SPI Behavior with Hazardous Access

The control register block uses an internal finite state machine that can only be initialized by the RST pin (asynchronous reset). When SPI access does not use 8 clock pulses, the internal finite state machine is desynchronized. The only way to resynchronize it is by resetting the sensor with the RST pin. No requester modification is recorded when a write access is made on a read-only register. Reliable initialization of read-only registers is not guaranteed when the slow SPI’s maximum clock frequency is not respected.

12. Control Interface (Slow SPI)

This interface controls the sensor’s internal registers. The protocol enables reading and writing of these registers.

The master (host) initiates transfers to the slave (sensor). The sensor can only use its interrupt pin to communicate with the host. When the host is interrupted, it must read the status register before continuing operation.

The word length of the transferred data is fixed to 8 bits. The Most Significant Bit (MSB) is sent first.

12.1 Communication Protocol

Accesses to the host are structured in packets of words. The first word is the command and the other words are the data.

The b7 bit is used to differentiate the command and data. When the word is a command, b7 is high (“1”) and when the word is a piece of data, b7 is low (“0”).

The following protocol is used:

12.1.0.1 Command Format

The host indicates to the sensor if it wants to read or write into a register and indicates the register's address.

b7	b6	b5	b4	b3	b2	b1	b0
1	Read (1)/Write (0)	Address (b3)	Address (b2)	Address (b1)	Address (b0)	x	x

12.1.0.2 Data Format (Writing into Register)

If writing into a register, the host transmits the data.

b7	b6	b5	b4	b3	b2	b1	b0
0	Data (b6)	Data (b5)	Data (b4)	Data (b3)	Data (b2)	Data (b1)	Data (b0)

12.1.0.3 Data Format (Reading of Register)

If reading a register, the host transmits one or several packets of data and data is shifted in from the sensor. The host transmits dummy words with the data format (b7 is low ["0"]). If reading the navigation or click pixel registers, the host transmits three packets of data to read the three registers.

b7	b6	b5	b4	b3	b2	b1	b0
0	x	x	x	x	x	x	x

Note: The host cannot communicate with the sensor without receiving data from it. Useless data is ignored by the host.

12.2 Communication Speed

To reduce consumption, the control interface's communication speed is set to the lowest possible speed and depends on the host's configuration.

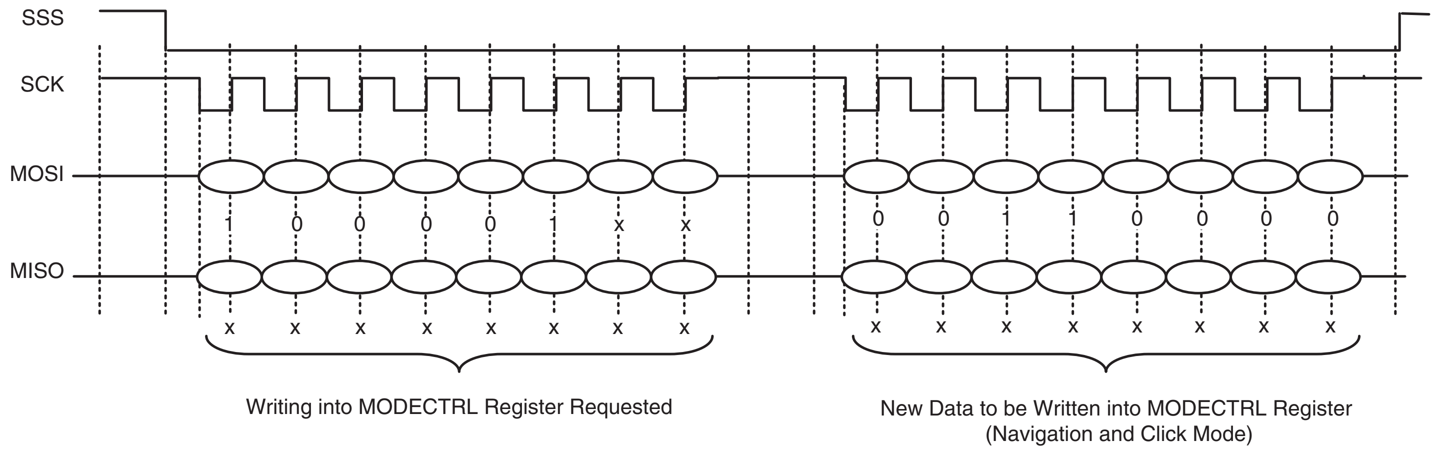
To communicate with "fast" controllers, the sensor's communication speed can be set to 200 kbits/s.

12.2.1 Example for the MODECTRL Register

Figure 10 represents a typical writing sequence into an internal register (MODECTRL register in this example).

See Appendix B for flowchart.

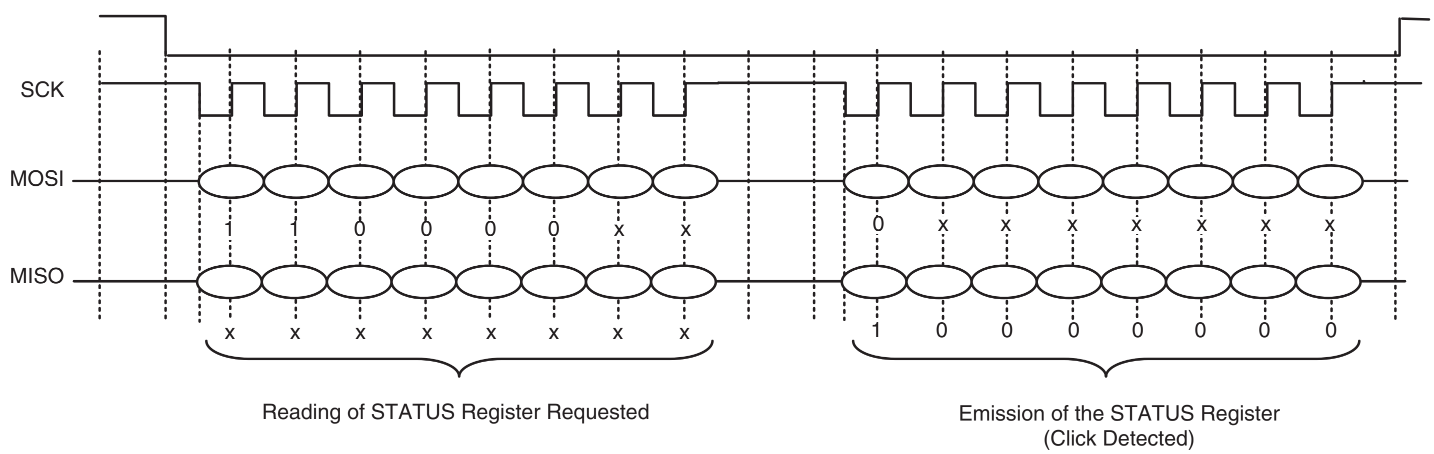
Figure 12-1. Writing into an Internal Register



Note: The break on SCK on the SPI chronogram has been added for better comprehension only. In a real application, SCK can be continuous.

Figure 11 represents a typical reading sequence of a register different from the navigation register. In this example, the status register is used.

Figure 12-2. Reading Sequence of a Register (Except for Navigation Registers)

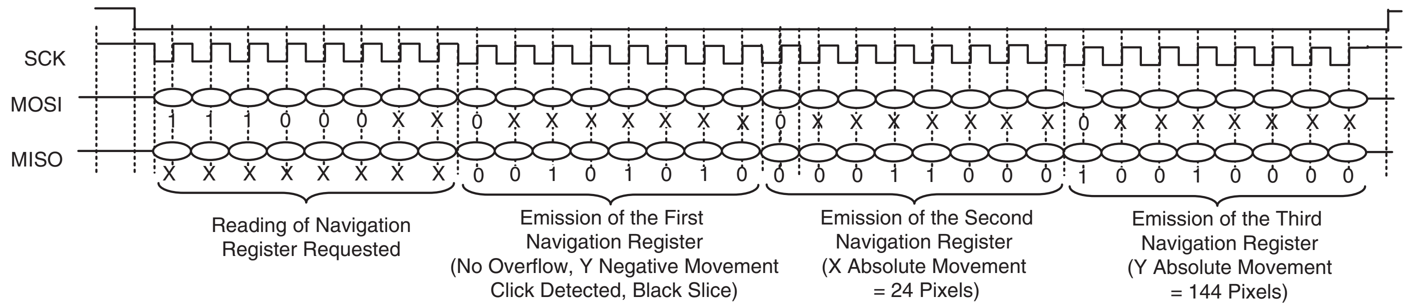


12.3 Example of Navigation Registers

Figure 12 represents a typical reading sequence of the three navigation registers.

Refer to ”Appendix C” on page 34 for flowchart

Figure 12-3. Reading of the Navigation Registers



13. Image Capture (Fast SPI)

This serial interface enables full-speed acquisition of the sensor's pixels by the host.

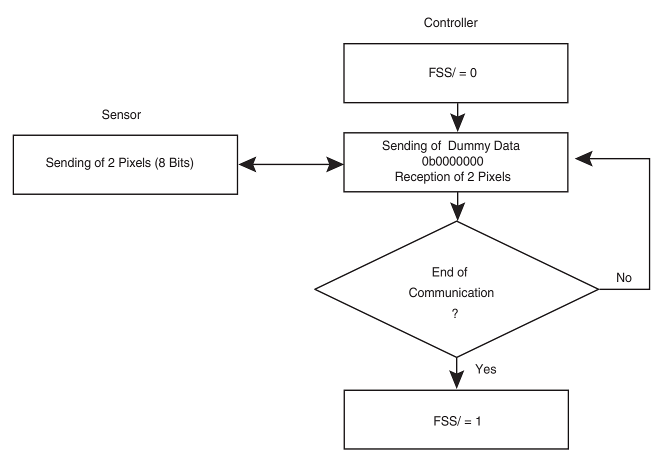
This interface only supports the serial clock (SCK) and one data line: MISO (Master In/ Slave Out).

13.1 Communication Protocol

When the sensor is in acquisition mode, the host can receive pixels through the fast SPI (FSS/ = 0). The host must transmit the communication clock (SCK) to receive the pixels. This clock must have a regular frequency to obtain constant fingerprint slices (See "Registration Integration Time" on page 26.).

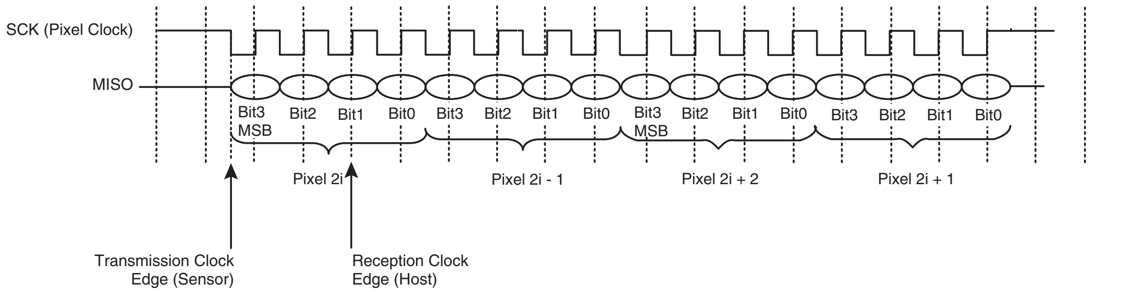
With the sensor configured to acquisition mode, the controller can proceed to fast accesses.

Figure 13-1. Example of an 8-bit Access



During an 8-bit access, the sensor transmits two pixels (each pixel is coded on 4 bits).

Figure 13-2. Fast SPI Communication



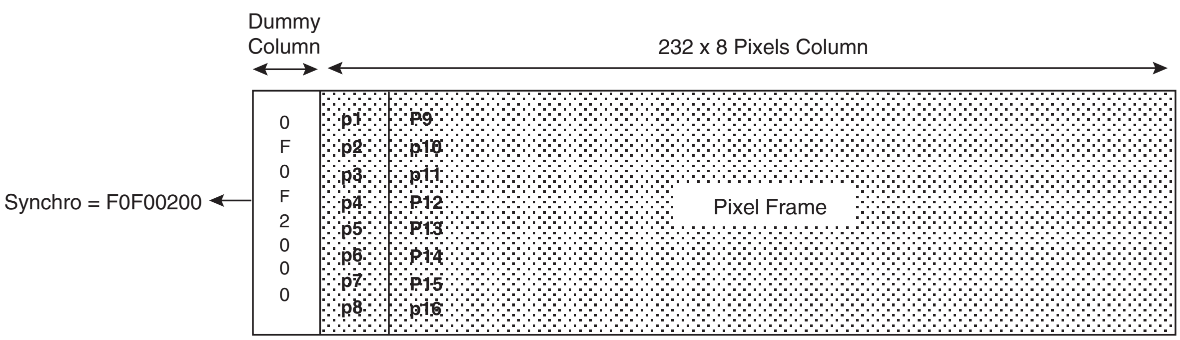
13.2 Communication Speed

The acquisition speed of the pixels is linked to the clock's communication speed. The faster the communication clock, the faster the authorized maximum finger sweeping speed. The sensor supports fast communications up to 16 Mbps.

13.3 Reading of Frame

A frame consists of 232 true columns and 1 dummy column of 8 pixels of 4 bits each. A frame starts with a dummy column.

Figure 13-3. Example of a Frame

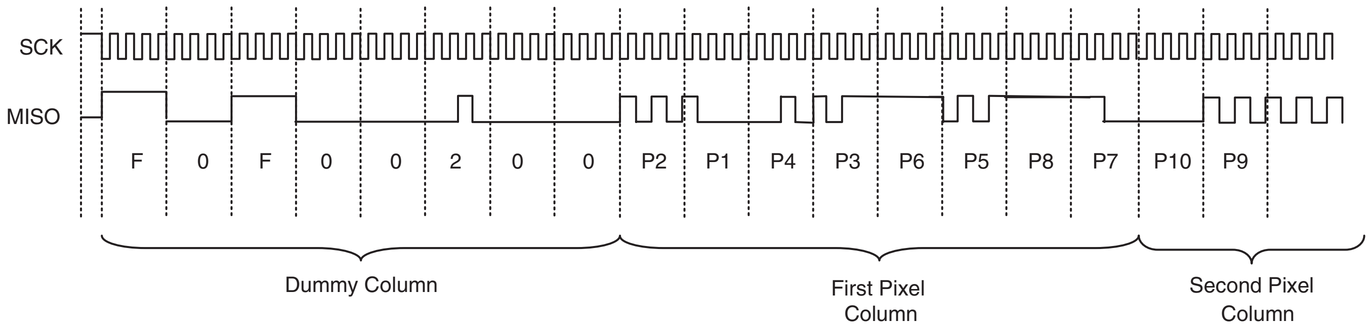


The first dummy column, at the beginning of the pixel array, is added to the sensor to act as a specific easy-to-detect pattern, and represents the start of the frame tag.

The pixel array is always read in the following order: the first byte, following the 4 bytes of the dummy column, which contains the value of the pixels physically located on the upper left corner of the array, when looking at the die with bond pads to the right. Then another 4 bytes are read that contain the value of the pixels located in the same column from top to bottom. The next column on the right is output, and so on, until the last line on the right, close to the bond pads, is output.

Even values are first sent during the data serialization for SPI transfer. Therefore, the synchronization sequence on the chip's MISO output is F0F00200.

Figure 13-4. Reading of Frame



Notes:
1. For the first array or frame reading, 40 dummy clock cycles must be sent before the first data arrives. This is necessary for the initialization of the chip pipeline. Consequently, the first synchronization sequences appear after 40 clock cycles. For the following array readings, data arrives at each clock cycle. One should implement a synchronization routine in the protocol to look for the F0F00200 pattern.
2. The Most Significant Bit (MSB) is sent first.

13.4 Reading of Entire Image

The FingerChip delivers fingerprint slices or frames with a height of 0.4 mm and a width of 11.6 mm (this equals 8 × 232 pixels). Pixels are sampled/read sequentially and are synchronous with SCK. Raw slices are captured by the acquisition system and overlapped with the corresponding X or Y finger displacement computed by Atmel reconstruction software. This reconstruction software supports a sweeping speed from 2 to 20 cm/s.

The table below shows finger speeds according to the different clock frequencies. The reconstruction results are obtained after acquisition of all slices.

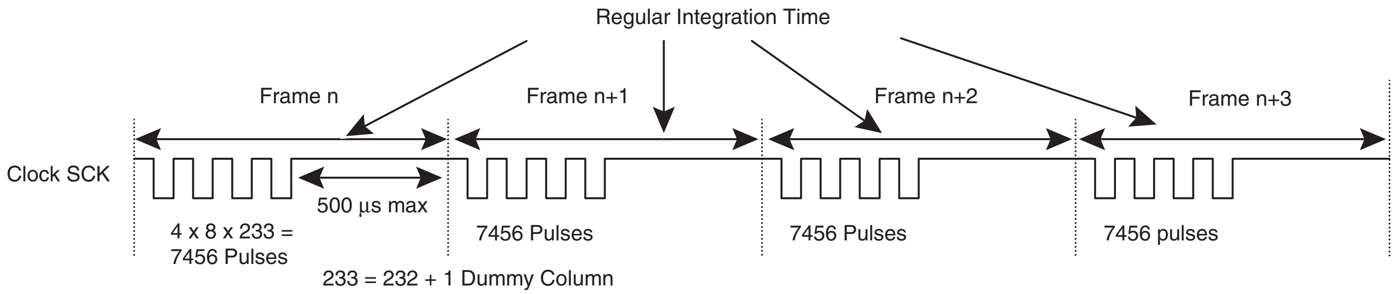
Table 13-1. Finger Speeds Versus Clock Frequencies

Fsck (MHz)	Data Rate (Mbit/s)	Slice Rate (Slices/s)	Absolute Maximum Finger Speed (cm/s)	Comments
1	1	134	3	Too slow
2	2	268	6	Too slow
4	4	536	12	Minimum
6	6	804	18	Normal speed
8	8	1072	24	Good speed
12	12	1608	36	Very good speed
16	16	2146	48	Very good speed

13.5 Registration Integration Time

The pixel’s integration time (the time needed for one frame reading) must be as regular as possible to obtain consistent fingerprint slices. This time is directly dependant on the SCK, SPI clock and frequency. Therefore, the SPI cycle of 4 × 8 × 233 clock pulses should be as regular as possible.µ

Figure 13-5. Regular Integration Time



Note: The 500 µs duration corresponds to the host's computation time (slice reconstruction, finger detection…) and in the illustration is given as an example only. Once the host detects a finger, this value remains constant, thus guaranteeing a regular integration time.

14. Navigation (Slow SPI)

The sensor's navigation function includes the processing elements necessary for providing the displacement of the finger touching the sensor in an up or down and right or left direction. It is aimed at a screen menu navigation or simple pointing application. In addition, a click processing function is embedded to detect a quick touch of the finger on the sensor. It is aimed at screen text, box or object selection. A double-click function could also be implemented in the software.

This interface has been designed to resemble the PS/2 mouse protocol.

An interrupt signal IRQ indicates to the host that an action has been detected. The host must read the status register to obtain details on the action. The IRQ signal enables implementation of an efficient power consumption protocol.

Note:

- Click and navigation modes can be used together.
- Two configurations are implemented for the click and navigation modes:
  – Stream mode, where the sensor sends an interrupt to the host when a movement or a change in the button's state is detected.
  – Remote mode, where the sensor does not interrupt the host but waits for its registers to be read.

  In these two modes, the registers are initialized after each reading from the host.

See "Appendix D" on page 35. for an example of an interrupt generated by a movement detection.

14.1 Navigation

See "Navigation Register" on page 17.

The typical navigation slice frequency has been fixed to 2.9 kHz. A programmable divider is implemented in the control registers (NAVFREQ) to reduce this frequency. Finger displacement is provided as a number of pixels in X and Y directions. Negative movements are possible. The register is cleared after the navigation registers are read. These registers are incremented or decremented between two accesses.

Table 14-1.

Navctrl Register (Bits b6 to b5)	Typical Navigation Slice Frequency (kHz)	Typical Integration Time (µs)	Typical Maximum Finger Speed (cm/s)
00	5.8	172	30
01	2.9	345	15
10	1.9	526	9.5
11	1.5	666	7.5

14.2 Click

See "Clickctrl Register" on page 16.

The sensor generates a click detection. The host must read the b7 bit of the status register or the b1 bit of the general navigation register.

The click function is composed of an array of a few pixels and a processing unit. The typical click slice frequency is 90 Hz. A programmable divider is implemented to modify this frequency in the control registers (CLICKFREQ).

14.3 Double-click

This function is performed by the controller, allowing better flexibility. It detects a succession of two clicks.

15. Temperature Stabilization Function and Watchdog

The sensor has an embedded temperature stabilization unit that identifies a difference in temperature between the finger and the sensor. When this difference is increased, the images are more contrasted. This function is optional and its use depends on the quality of the image processing software, therefore its management should be decided together with the image processing software.

In order to limit excessive current consumption by the use of the temperature stabilization function, a watchdog has been implanted in the sensor. The local oscillator stops the heating of the module after a defined time. The oscillator should not be stopped as long as watchdog is active, otherwise the clock stops automatically.

When heating of the sensor is requested "1" is written in bit 6 of the HEATCTRL register) and the watchdog is enabled "1" is written in bit 5 of the HEATCTRL register), the sensor is heated during 'n' seconds.

Due to the oscillator frequency dispersion, the value of n is:

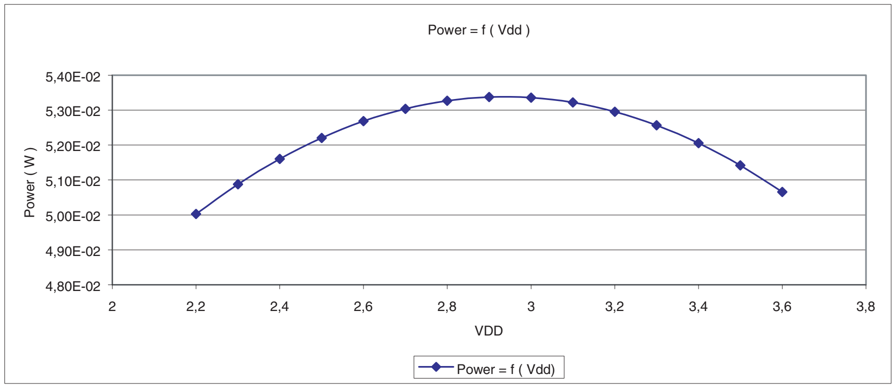
2 seconds (minimum) < n = 4 seconds (typical) < 7 seconds (maximum).

The accuracy of n is not important since the heat register can be enabled successively.

The level of power consumption is programmable. Two pre-programmed values are set to 50 or 100 mW.

The dissipated die power is quasi constant over a significant supply voltage range as shown below (mode 50 mW selected):

Figure 15-1.



Note: This function is useless for navigation and click modes.

16. Power Management

16.1 Sleep Mode (<10 µA)

Reset high

16.2 Standby Mode (<10 µA Providing SPI Bus not Accessed)

Power consumption can be reduced in several ways:

- By switching off the FingerChip sensor.
- By programming a standby mode by writing 00001xx in the MODCTRL register (STANDBY mode set and oscillator stopped.) Bit b6 (HEAT) of the HEATCTRL register must be turned to ‘0’ when programming standby mode.

16.3 Acquisition Mode Current Consumption

16.3.1 Static Current Consumption

When the SPI bus is not used, only the analog part of the circuit consumes power at around 4 mA.

16.3.2 Dynamic Current Consumption

When the clock is running, the digital sections also consume current. With a 30 pF load at 16 MHz, the power consumption is approximately 4.5 mA on the V_{DD} pins.

16.4 Navigation and Click Modes Current Consumption

16.4.1 Static Current Consumption

The SPI bus' consumption is very low in click and navigation modes, the majority of the consumption being generated by the analog part of the circuit. Therefore, the static and dynamic consumption is almost the same.

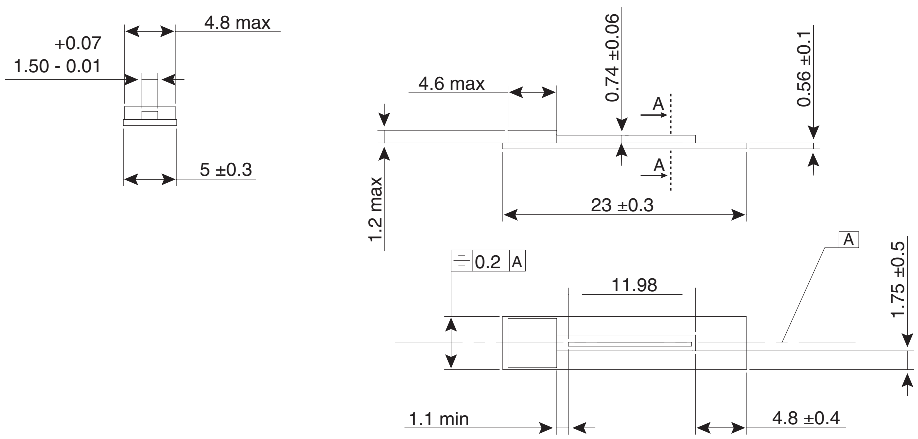
16.4.2 Dynamic Current Consumption

With a 30 pF load at maximum clock frequency, the current consumption in click mode is almost 300 µA on pins V_{DD}. With a 30 pF load at maximum clock frequency, the current consumption in navigation mode is approximately 1.5 mA.

Note: We advise use of the interrupt capabilities (IRQ signal or Interrupts register) so as to limit the host's overall current consumption. The host can, from time to time, check the IRQ or Interrupt register. A strategy for very low power consumption is to use the click mode only as a wake-up. The click mode is only 300 µA, and once a click is detected the host can turn on the navigation mode as well.

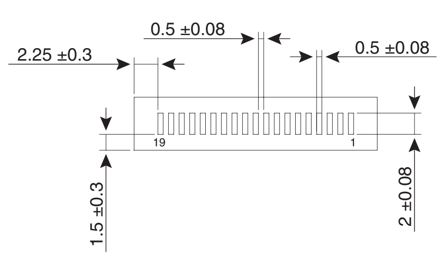
17. Packaging Mechanical Data (values to be confirmed)

Figure 17-1. AT77C105A-CB08YV Top View



Note: All dimensions in mm.

Figure 17-2. AT77C105A-CB08YV Bottom View



Note: All dimensions in mm.

17.1 Package Information

17.1.1 Electrical Disturbances

Three areas of the FingerChip device must never be in contact with the casing, or any other component, so as to avoid electrical disturbances. These areas are shown in Figure 17-3:

Figure 17-3. Sensitive Areas

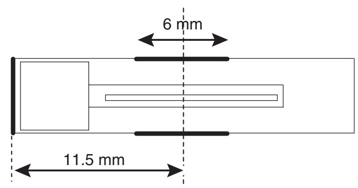
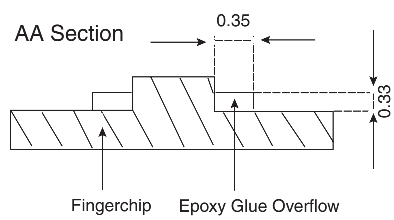


Figure 17-4. Epoxy Overflow

Maximum epoxy overflow width: 0.35 mm on the die edge.

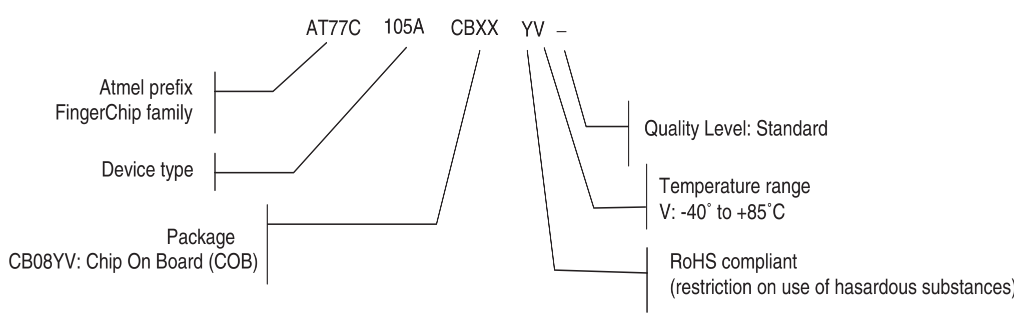
Maximum epoxy overflow thickness: 0.33 mm.



Note: Refer to Figure 17-1 on page 30.

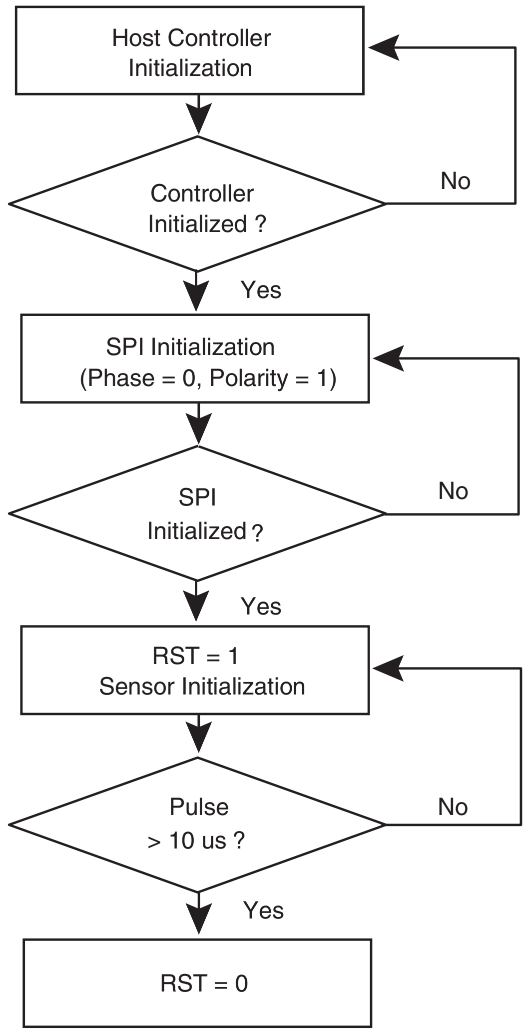
18. Ordering Information

18.1 Package Device



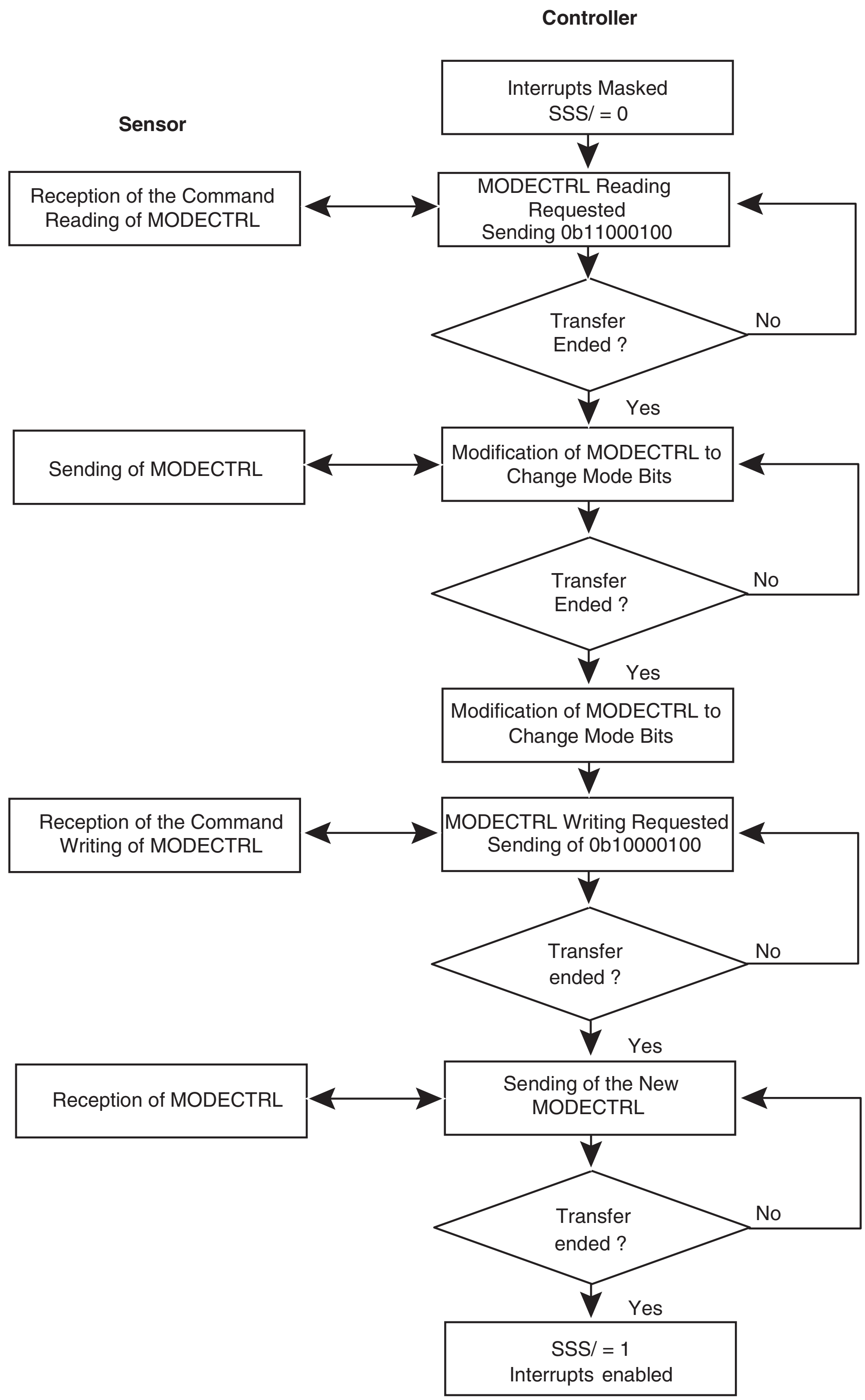
19. Appendix A

19.1 Controller Initialization



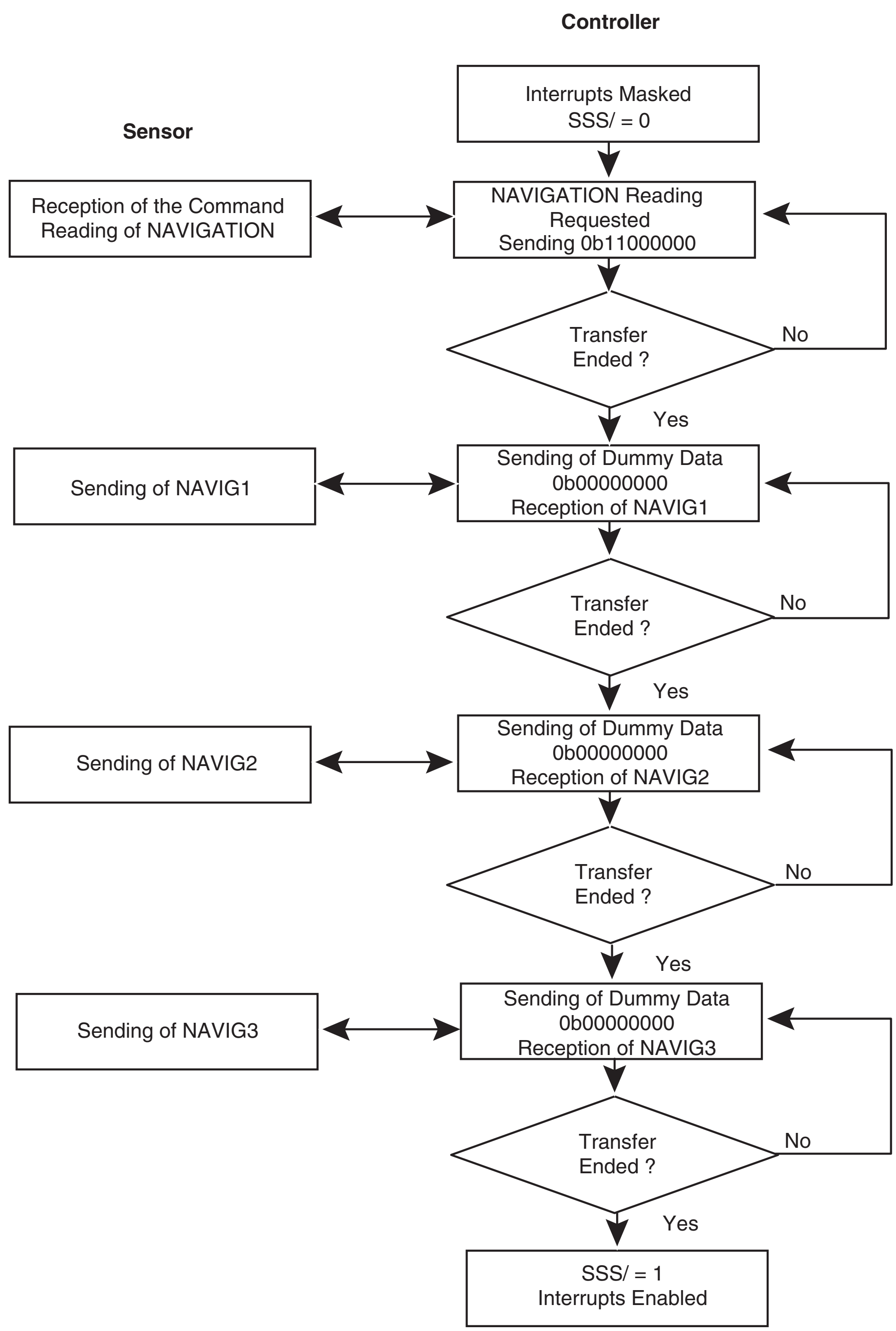
20. Appendix B

20.1 Example for the MODECTRL Register



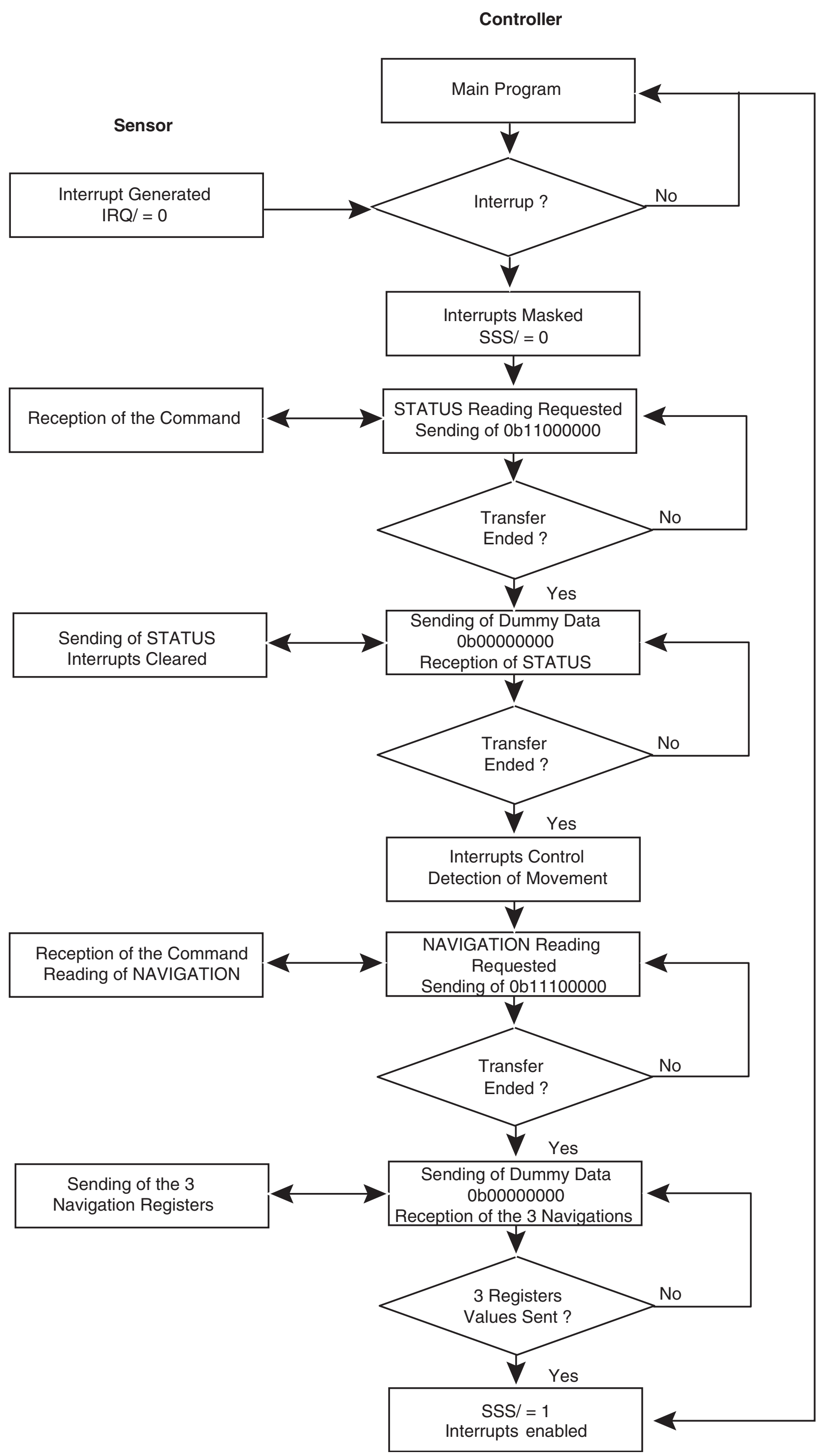
21. Appendix C

21.1 Example of Navigation Registers



22. Appendix D

22.1 Example of an Interrupt Generated by a Movement Detection



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