Features

- Thermal Sensing technology
- Image zone: 0.3 x 9.6 mm^2
- Image array: 6 x 192 = 1152 pixels
- Image resolution: 508 dpi (50 µm x 50µm pixel pitch)
- Universal Serial Bus (USB) 2.0 Full-Speed, bus powered
- Serial Peripheral Interface (SPI) for optional serial flash support
- Operating voltage range: 3.0V to 3.6V
- Operating Temperature Range: -40ºC to 85ºC
- Finger Sweeping speed from 2 to 25 cm/Second
- High on-chip security features: Data encryption and challenge response, fake finger detection.
- Low Power Mode: Image acquisition, click & navigation, Wake up, Suspend, Stand By.
- Small Form Factor Molded Packaging
- High Protection from Electrostatic Discharge: +/-16 kV
- Resistance to abrasion: >20 millions finger sweeps
- RoHS Compliant

Description

Combining superior thermal sensing technology with field-proven USB IP, the AT77C109 is a single chip USB fingerprint sensor designed specifically for the PC and PC-like applications with the lowest BOM cost and easiest integration path.

Atmel's thermal technology enables superior image acquisition under very difficult finger conductions such as wet, dry and greasy fingers. It leads to enhanced end user experience in terms of lower false reject rate (FRR).

The inclusion of the fake finger feature based on the skin electrical properties measurement enables non-living tissues rejection and protection.

This sensor also embeds a processor providing encrypted biometrics operation in a highly secured environment protecting user's privacy.

The AT77C109 comes in innovative molded package. Its hard plastic surface is designed to ensure long operating life of the sensor in harsh environment against abrasion, chemical erosion and other user abuses. The symmetric, flat shape of the sensor enables simple mechanical integration into space constrained devices.

The non-conducting surface of the sensor, along with a ground titanium electrode layer inside the sensor, provides ESD protection of up to 16 kV. It allows for lowest overall BOM cost and simpler manufacturing support.

The AT77C109 boasts 4 operating modes, including acquisition, navigation and click, wake-up, and suspend mode to ensure the lowest power consumption in various usage scenarios.

The AT77C109 is supported by Atmel biometrics software development kit (SDK) and biometrics application suite from biometrics software.

Applications

- Notebooks
- PC peripherals
- UMPC
- POS
- Other devices requiring USB interface

Security Thermal Fingerprint sensor with Universal Serial Bus (USB) 2.0 Full-Speed interface

Acquisition
Navigation
Wake up
Fake Finger
Memory Bridge
Suspend functions

AT77C109A

Preliminary Datasheet

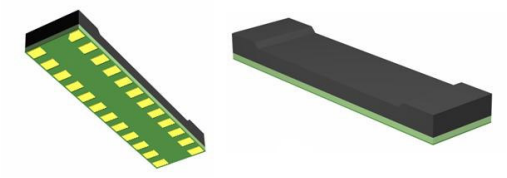
XXXXA–XXXX–XX/XX

1. Molded Package

The molded package provides a symmetric, thin profile design ideal for integration in space constrained devices such as notebooks. It also allows better protection against various environmental elements such as chemical erosion, scratch, abrasion, etc.

Mechanical integration guideline is available from Atmel to ensure the most ergonomic finger guide for maximum FingerChip sensor performance.

Figure 1-1. Molded Package for AT77C109A



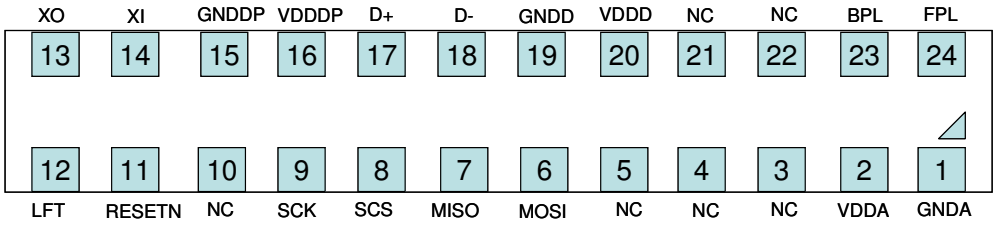
2. Pin Description

Table 2-1. Pin Description for molded Package: AT77C109A-ZD01YV

Pin Number	Name	Type	Description
1	GNDA	P	Analog Ground
2	VDDA	P	Analog Power Supply
3	-	-	NC
4	-	-	Reserved (left unconnected)
5	-	-	Reserved (left unconnected)
6	MOSI	output	memory bridge data out
7	MISO	Input, pull up	memory bridge data in
8	SCS	output	memory bridge chip select (active high by default)
9	SCK	output	memory bridge serial clock
10	-	-	Reserved (left unconnected)
11	RESETn	Input, pull up, S trigger	External reset (Optional)
12	LFT	I/O	PLL low pass filter
13	XO	O	12 MHz quartz oscillator
14	XI	I	12 MHz quartz oscillator
15	GNDDP	P	PLL + OSC Ground
16	VDDDP	P	PLL +OSC Power Supply
17	D+	I/O	USB pad
18	D-	I/O	USB pad
19	GNDD	P	Digital Ground
20	VDDD	P	Digital Power Supply
21	-	-	Reserved (left unconnected)
22	-	-	NC
23	BPL	P	Must be connected to FPL
24	FPL	P	Must be connected to BPL

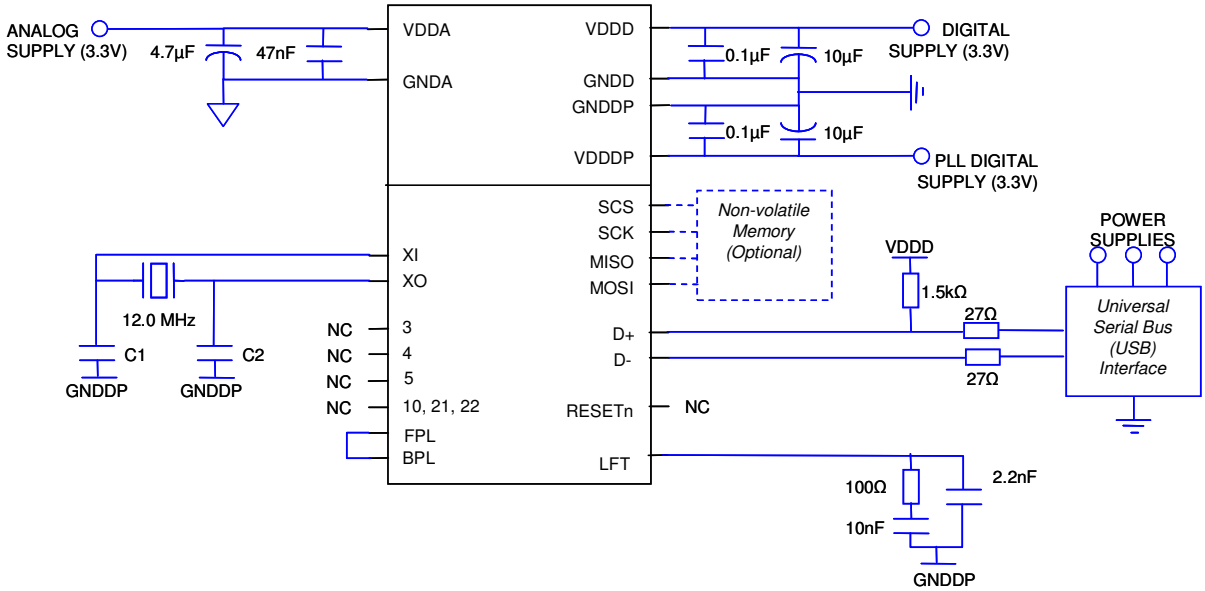
Note: The die attach is connected to GNDA and must be grounded. The FPL pin must also be grounded.

Figure 2-1. Pin description from Bottom View



3. Typical Application

Figure 3-1. Typical Connection Diagram



Note: The noise must be lower than 30 mV peak-to-peak on the analog and digital power supply.

4. Specifications

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value
Power supply voltage	V_{DDD}, V_{DDA}, V_{DDDP}		-0.5 to 4.6V
Front Plane	FPL		Connected to BPL
Digital Input	XI, LFT, RST, MOSI		G_{NDD} to V_{DDD}+0.5V
Storage temperature	Tstg		-40 to +85°C
Lead temperature	Tleads		130°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	V_{DD}	V_{DD}=V_{DDD}=V_{DDA}=V_{DDDP}	3	3.3	3.6	V
Front plane	FPL	Must be connected to BPL	BPL			V
Digital input voltage			CMOS levels			V
Digital output voltage			CMOS levels			V
Digital input voltage	D+, D-		USB 2.0 compliant			
Digital output voltage	D+, D-		USB 2.0 compliant			
Digital load	C_L			20	50	pF
Operating temperature range	T_{amb}	Industrial	-40 to +85			°C
12 MHz resonator	Q	crystal precision			50	ppm

Table 4-3. Environmental Resistance

Parameter	Min value	Standard method
ESD		
On pins. HBM (Human Body Model) CMOS I/O	2 kV	MIL-STD-883- method 3015.7
On die surface (Zap gun) Air discharge Contact discharge	 +/- 16 kV +/- 8 kV	NF EN 6100-4-2
MECHANICAL ABRASION		
# Cycles without lubricant Multiply by a factor of 20 for correlation with a real finger	1 000 000	Internal method
CHEMICAL RESISTANCE		
Various tests with aggressive chemical agents		Internal method

Table 4-4. Explanation of Test Levels

Level	Description
I	100% production tested at +25°C
II	100% production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample)
III	Sample tested only
IV	Parameter is guaranteed by design and/or characterization testing
V	Parameter is a typical value only
VI	100% production tested at temperature extremes
D	100% probe tested on wafer at T_{amb} = +25°C

Table 4-5. Specifications

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Resolution		IV		50		Micron
Size		IV		6 × 192		Pixel
Yield: number of bad pixels		I			5	Bad pixels

5. Power Consumption and DC Characteristics

The following characteristics are applicable over the operating temperature range. Testing conditions are: power supply = 3.3V; Tamb = 25°C; Fcrystal = 12 MHz (active mode); duty cycle = 50%;
CLOAD 20 pF on digital outputs unless otherwise specified.

Table 5-1. Power Requirements

Name	Parameter	Conditions	Test Level	Min	Typ	Max	Unit-
V_{DD}	Positive supply voltage	$V_{DD}=V_{DDD}=V_{DDA}=V_{DDDP}$	I	3	3.3	3.6	V
I_{SUSP}	USB suspend mode		I			80	µA
I_{STB}	Stand By		I		15		mA
I_{MEM}	Memory Bridge mode		I		20		mA
I_{DDACQ}	Acquisition mode		I		30		mA
I_{DDNAV}	Navigation mode		I		25		mA
I_{DDWU}	Wake up mode		I		60	100	µA
I_{TEST}	Test Mode	Test Mode On	I			80	mA

Table 5-2. Digital Inputs

Logic Compatibility		CMOS					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
I_{IL}	Low level input current without pull-up device	V_I = 0V	I			1	µA
I_{IH}	High level input current without pull-down device	$V_I = V_{DD}$	I			1	µA
I_{ioz}	Tri-state output leakage without pull up/down device	V_I = 0V or V_{DD}	IV			1	uA
V_{il}	Low level input voltage		I			0.3 Vdd	V
V_{ih}	High level input voltage		I	0.7 Vdd			V
V_{hyst}	Schmitt trigger hysteresis	V_{DD} = 3.3V Temp = 25°C	IV	0.40		0.75	V

Table 5-3. Digital Outputs

Logic Compatibility		CMOS					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Low level output voltage	I_{OL} = 3 mA V_{DD} = 3.3V ±10% I_{OL} = 1.75 mA V_{DD} = 2.5V ±5%	I			0.15 V_{DD}	V
V_{OH}	High level output voltage	I_{OH} = -3 mA V_{DD} = 3.3V ±10% I_{OH} = -1.75 mA V_{DD} = 2.5V ±5%	I	0.85 V_{DD}			V

6. Switching Performances

The following characteristics are applicable over the operating temperature range. Testing conditions are: power supply = 3.3V; Tamb = 25°C; Fcrystal = 12 MHz (active mode); duty cycle = 50%;
C_{LOAD} 20 pF (tester load) on digital outputs unless otherwise specified.

Table 6-1. USB Timings

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Clock frequency	Fcrystal	IV		12		MHz
Duty cycle (clock SCK)	DC	IV		50		%
Universal Serial Bus	D+/D-	IV	USB 2.0 compliant			ns

Table 6-2. SPI Timings

Parameter	Symbol	Test Level	Min.	Typ.	Max.	Unit
Clock frequency	FSCK	IV			12	MHz
Duty cycle (clock SCK)	DC	IV	20	50	80	%
SCK falling edge to MOSI delay	Tpmosi	IV	0.0		6.0	ns
MISO to SCK setup time	Tsumiso	IV	7			ns
MISO from SCK hold time	Thmiso	IV	0			ns

Note: See **Table 14-1.** For SPI mode configuration

6.1. Blocks start sequence in the chip

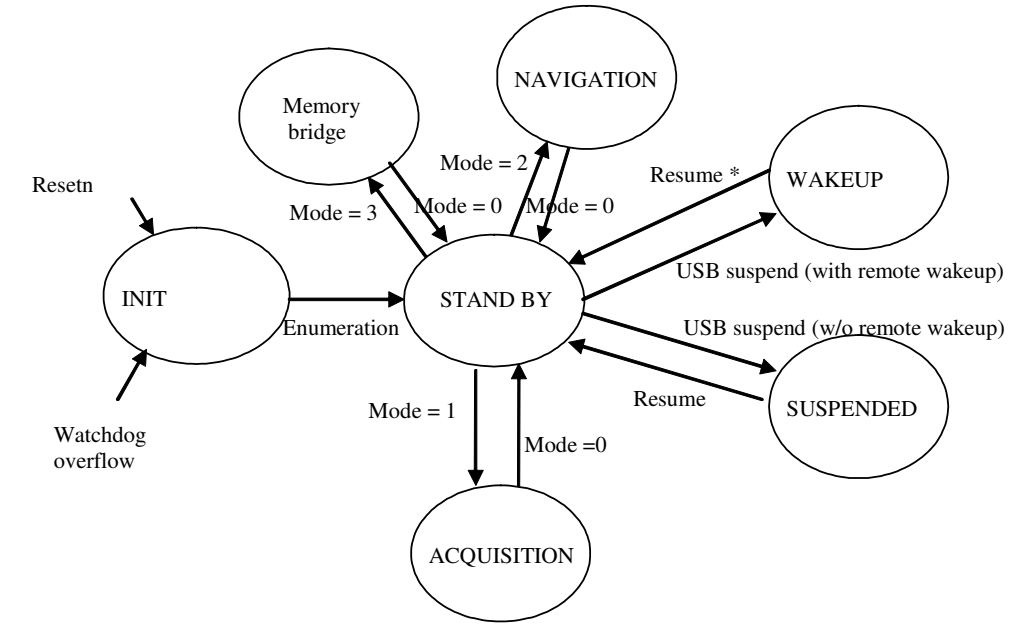
POR: a Power on Reset is necessary for the chip to start correctly. The hard reset is done through the USB power wires, so the USB function is reset by the POR at the device connection. Reset duration is maximum 10 µs.

6.2. Reset description

POR: Power on reset is a hard reset of the entire chip after USB power connection.
RSETN: RSETN external pin is a hard reset of the entire chip, dedicated to the test mode (USB hard reset can not be used in test mode).
USB Reset command: partial reset; all functions are reset except USB.
Reset Vendor Command: set the control register with default values, put the At77C109 in idle mode and wait for the USB command.

7. Functional Description

Figure 7-1. Architecture – State Machine



* : USB downstream resume or remote wakeup

AT77C109A is a fingerprint sensor based on FingerChip® technology. It is controlled by an USB interface.
Six modes have been implemented:

Start Sequence/Stand by mode
Power On Reset and USB reset force FC109 in INIT mode. The Reset input can be used to force a reset pulse longer than the internal power on reset.

Acquisition mode
In this mode, fingerprint slices are transferred directly to the host for biometric purposes. The full 192 x 6 pixel array is used.
Slices are transferred within maximum size bulk USB packets (64 bytes, i.e. 128 pixels in bulk mode, 585 bytes in isochronous mode).
In bulk mode, each slice is split into 10 packets: 9 full packets for the pixel array and a short stop packet are providing the synchronization words to the host.
In isochronous mode, a slice is transmitted in one or two packets, depending on the system bandwidth available.
Fingerprint reconstruction is implemented by USB host at the driver or application software level.

As regular as possible acquisition is recommended to get high quality fingerprint images. It is recommended to pipe as many slices requests as possible to get the fastest access to USB bandwidth in bulk mode. Isochronous mode may be implemented to lock integration time when USB line is share and heavily loaded.
Host can interrupt acquisition at any time by sending an idle request on EP0.

Navigation & click mode
In this mode, reduced fingerprint slices are transferred directly to the host for navigation purposes.

A small 128 x 6 pixel array is used, to reduce power consumption, speed up array reading and ease finger tracking (although full speed sampling is less critical than in acquisition mode).
Slices are transferred within maximum size bulk USB packets (64 bytes, i.e. 128 pixels). Each slice is split into 7 packets: 6 full packets for the 128 x 6 pixels and a stop packet providing synchronization words. Isochronous mode transfers slices in 1 packets/frame.

Navigation raw data may be managed at the driver layer or pushed to the application software if required for further processing.

Host can interrupt navigation at any time by sending an idle request on EP0.

Wake Up detection
Very low power consumption is possible thanks to wake up mode.
The sensor is able to detect a finger swipe, and generate a remote (upstream) wakeup. It will enter wakeup mode upon detection of USB suspend condition, if it was previously allowed to do so: the host system should arm the wakeup mode by sending a “set feature” token. Then already in stand-by mode, enters in Wakeup mode upon USB suspend event, and may be waken in a user friendly way by a finger sweep.

Wake up makes use of a dedicated pixel array and a slow internal clock. This mode does not generate any image but it can be followed by an immediate slices acquisition.

A downstream wakeup or an USB reset from host will force FC109 to return to stand by mode.

Memory bridge mode

This feature will be used to drive a local storage media to store credentials and biometric templates, for instance.
FC109 WILL NEVER DECLARE ITSELF AS AN USB STORAGE DEVICE.

FC109 bridge mode provides transparent access to a non volatile memory.
FC109 interfaces only with standard SPI flash or e2prom memories. Protocol layers must be managed by software. Any secure mechanism should be implemented at the host level (driver or application software).

FC109 does not implement any address or data checking (page boundary, protected areas…). Up to 256 bytes may be read at time from memory according to the USB request. Only 8 bytes bursts can be written to, owing to the FC109 limited buffer memory. Transfer parameters include: number of instruction+address bytes, number of data bytes, and direction of transfer (after the instruction/address bytes). Busy signaling on data line is not supported.

Before sending the read or write interrupt, user has to setup the SPI request header: instruction + start address (1 + 4 bytes). The “memory setup” USB instruction has been defined for that purpose. Upon reception of the custom “memory read/write” instruction, MCU will send the setup data to the non volatile memory, then send write or fetch the requested byte number. Read data are then returned to host after the next IN token.

7.1. On-chip Security features

Fingerprints are used to protect electronic data and devices. In order to secure transactions between the system and the sensor, a security engine has been implemented in the FC109 with the following features:

Data encryption
FC109 is able to encrypt the data flow upon request of the host processor.

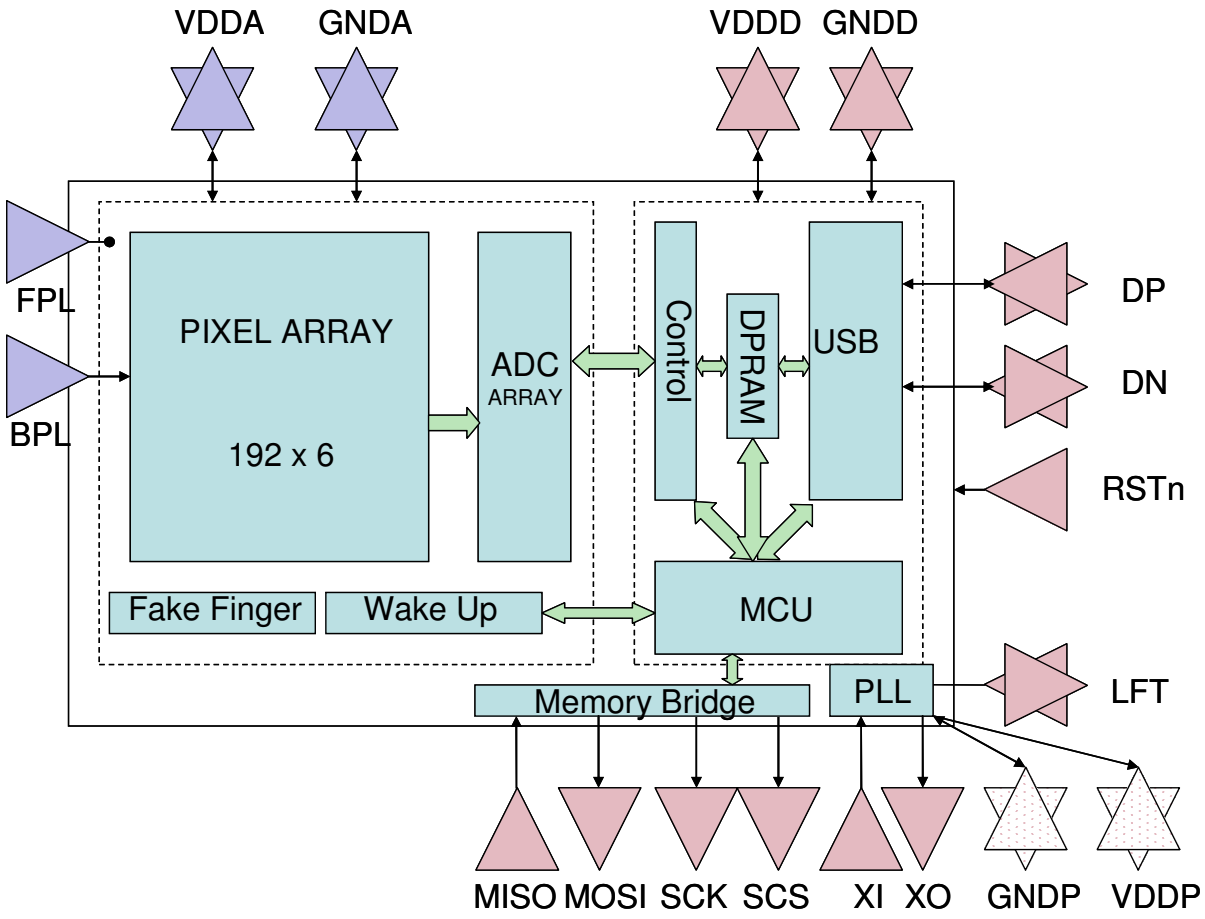
Challenge response
Host and FC109 exchange challenges and responses to enable hardware authentication.

Fake finger detection
In order to reduce fraud, a fake finger detection system may be triggered. Two external electrodes monitor finger characteristics that are used to sort true living fingers and fake fingers.

Note: Contact ATMEL for further details about these features.

8. Sensor and Block Diagram

Figure 8-1. Functional Block Diagram



The Circuit is divided into the following main sections:

- Pixel array or frame of 6 x 192 pixels +1 dummy column
- Analog to digital conversion
- control & interface mode (CPU + USB IF)
- Wake up
- Fake finger detection
- serial interface (memory bridge)

9. USB Interface General Description

Functional behavior:

Every functional action is under USB control.
Three USB endpoints are required for the device (at most 2 are active simultaneously):

endpoint	mnemonic	size	fifo banks	type	direction
0	EP0	8	1	control	in
0	EP0	8	1	control	out
1	EP1	64	2	bulk	out
2	EP2	585/297	-	isochronous	out

USB functional control and enumeration requests are transferred to the MCU through EP0. Custom vendor commands are used to manage modes.
An internal watchdog runs during active modes. Overflow will reset the internal logic and return stall on next USB request.

10. IMAGE CAPTURE

Sensor description

Every pixel acts as a local temperature sensor. This sensor is able to detect a temperature difference between two readouts: this delay is referred to as the integration time.
Owing to the thermal properties of the sensor coating, electrical charges are generated at a rate depending on the temperature variation during the integration delay. The resulting voltage also depends on the duration of this phase, which has a typical value of 1 millisecond.

Analog to Digital Converter

A single ramp Analog-to-Digital Converter (ADC) is used to convert the amplified analog signal from the pixels into 4 bits words.

Definition of fingerprints slices

A slice consists in 192 columns of 6 pixels, digitized on 4 bits (it is sometimes referred to as frames, not to be mistaken with USB frames).

A 9 bytes synchronization stop sequence is used at the end of each slice. This sequence is used by USB as end of slice packet, and by driver/application software to verify integrity of incoming data.

Slices transfer

AT77C109 is a slave device. All transfer operations are conducted upon request under USB host supervision. Isochronous transfer deliver 4.7 Mb/s. Bulk transfers may reach up to 11.7 Mb/s.

10.1. Image transfer protocol

FC109 makes use of USB bulk transfer by default. This mode ensures safe data transfer at the penalty of potentially reduced bandwidth when the line is share with other devices, and it is supported by any host –even in pre-boot mode-.
USB is a half duplex bus that uses packet-based exchanges of tokens, commands or data. Bulk packets are limited in size, but FC109 will use the maximum sized packets of 64 bytes to minimize the protocol overhead.

The high level USB protocol is managed by firmware running on an embedded MCU. Image data are transferred directly by the array control logic to the USB FIFO to release the MCU from high throughput data management.
At application/pipe level, atomic FC109 data transfer is a slice, which means that bulk USB request must ask for 585 bytes. The FC109 will deliver 9 packets of 64 bytes that hold 6 x 189 x 4 bits = 2,560 useful bits and a 10^{th} packet containing the remaining pixels and synchronization bytes. This short packet flags the end of the slice to the USB host. The navigation mode makes use of a reduced slice of 7 packets.

Isochronous mode behavior is slightly different. Only one packet per frame is allowed. According to fair bandwidth allocation, host allows FC109 to deliver full slice or half slice packets. Like bulk packets, the final slice packet will hold synchronization data.

10.2. Slices mapping in USB framework

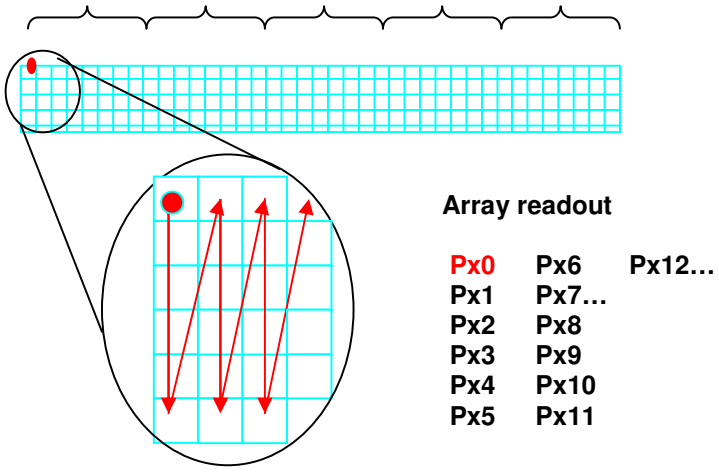
The pixel array is transferred column by column from the upper left corner of the array (looking at the die with FPL bond pads to the bottom right) to the lower right corner. Column pixels are transferred from top to bottom (using the same convention). For each byte, the 4 most significant bits are the lower pixel converted value, and the 4 least significant bits are the upper pixel converted value. A packet contains 21 columns, that is 63 bytes and a packet filler (= packet number from 9 down to 0) PK0 holds the last 3 columns, and slice filler data (see below).

Figure 10-2-1 Content of an USB Byte

MSB= Px1(3) Px1(2) Px1(1) Px1(0) Px0(3) Px0(2) Px0(1) Px0(0) *=lsb*

USB Packets (full array, acquisition mode, bulk):

	Pk9	**Pk8**	**Pk7**	**Pk6**	**Pk5**	**...**	***Pk0***
B0	Px1Px0	Px127..	Px253…	Px379…	Px505…	…	*Px1135 … 1151*
B1	Px3Px2	…	…	…	…	…	*F0h*
B2	Px5Px4	…	…	…	…	…	*F0h*
B3	Px7Px6	…	…	…	…	…	*fc*
B4	Px9…	…	…	…	…	…	-FC
…	…	…	…	…	…	…	-(ff)
B63	00/FFh	01h	02h	03h	…	…	-



Pixels reading and packing

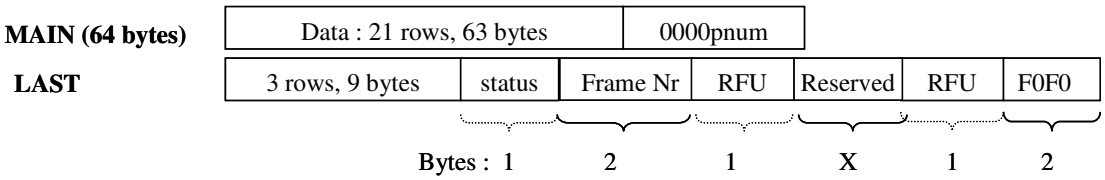
Alternate interfaces, acquisition mode
In order to ensure a regular integration time, alternate interfaces may be configured for isochronous USB data transfer. Two alternate settings are selectable to deal with the USB available bandwidth: 585 bytes packets (1 slice / USB frame, 1 ms fixed integration time) and 297 bytes packets (1/2 slice per USB frame, 2 ms fixed integration time).
Packets are organized in the same order as bulk packets. After the last pixels the slice filler (described below) is inserted. In ½ slice per frame, pixels 0 to 575 (col95) lay in even frames and pixels 576 to 1151 lay in odd numbered frames.

Navigation mode
Navigation scans a reduced pixel array from pixel 128 to pixel 511 (columns 32 to 127). These pixels are organized in 7 USB packets, 6 pixels packets equivalent to acquisition PK7 to PK2 and a stop packet similar to acquisition PK0. They are numbered from 6 to 0.
Isochronous USB data transfer is available in this mode. The USB bandwidth available is: 390 bytes packets (1 slice / USB frame, 1 ms fixed integration time).
Packets are organized in the same order as bulk packets. After the last pixels the slice filler (described below) is inserted.

Packets and End of slice filler structure according to mode

Bulk mode
For obvious reasons, last packets synchro and other filler data are not encrypt.

Figure 10-2-2 Bulk mode

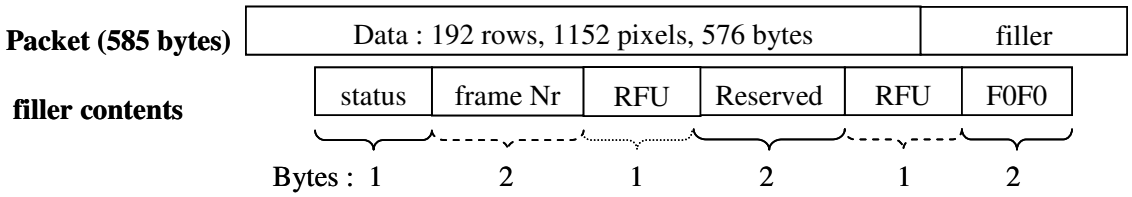


Status : PIX_TEST_1 : PIX_TEST_0 : X : X : X : X : 0 : 0
Frame number : (4 bits free running) slice counter : 0 : USB frame number (11 bits)

Isochronous mode

For obvious reasons, last packets synchro and other filler data are not encrypt.

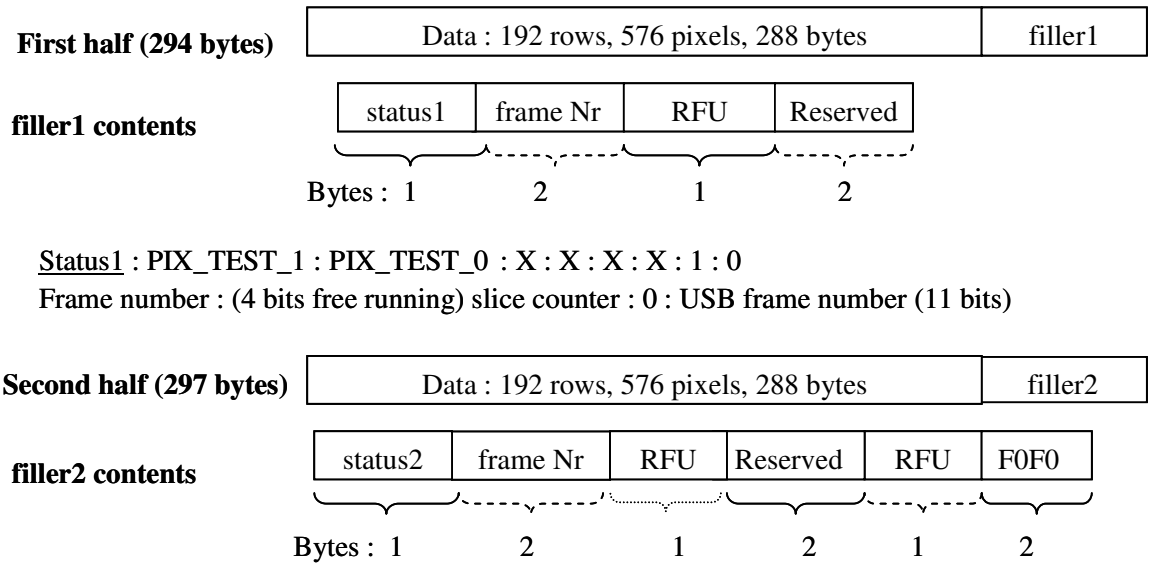
Figure 10-2-3. Isochronous mode (standard)



Status : PIX_TEST_1 : PIX_TEST_0 : X : X : X : X : 0 : 0

Frame number : (4 bits free running) slice counter : 0 : USB frame number (11 bits)

Figure 10-2-4. Isochronous mode (reduced data rate)



Status1 : PIX_TEST_1 : PIX_TEST_0 : X : X : X : X : 1 : 0

Frame number : (4 bits free running) slice counter : 0 : USB frame number (11 bits)

Status2 : PIX_TEST_1 : PIX_TEST_0 : X : X : X : X : 0 : 0

Frame number : (4 bits free running) slice counter : 0 : USB frame number (11 bits)

11. Control interface

Control tasks are executed by MCU. This includes managing USB protocol, such as enumeration, commands extraction.
Transfers are always initiated by USB host to the device (FC109 MCU). Control (read and write) flows through end point EP0. Excluding remote wakeup mechanisms, no upstream request is implemented in FC109.
The atomic transfer unit is the USB packet, either setup, acknowledge or data.

Registers access
Registers are accessed using USB vendor commands described in the **Table 11.1** below.

Table 11-1. Vendor commands definition for FC109

Request	Type	Recipient	Dir.	bRequest	Value	Index	Count	Description
Reset	42h	EP0	W	82h	0000h	0000h	0000h	Reset sensor (except MCU)
Set mode	42h	EP0	W	82h	0020h	000mh	0000h	Change functional mode
memory setup	42h	EP0	W	82h	000Ah	0000/1	N	Setup memory xfer: instruction + address bytes
Write cfg Reg	42h	EP0	W	82h	0003h	0@rrh	0000h	Write configuration register
Read cfg Reg	C2h	EP0	R	82h	0004h	0@00h	0001h	Read configuration or status register
Read mem. access	C2h	EP0	R	82h	0008h	0000h	N	Read N data from memory from latest setup address
Write mem. access	42h	EP0	W	82h	0009h	0000h	N	write N data into memory from latest setup address
Get Version	C2h	EP0	R	82h	0010h	0000h	0002h	Read a structure grouping respective versions numbers of chip and firmware
RFU	-	-	-	82h	others	-	-	Reserved

Where:

@ Stands for register number, (see register description).
rr Stands for register new value
m Stands for mode value: (see register description).
Other Values (instructions codes) are reserved and may not be used.

Fingerprint interface

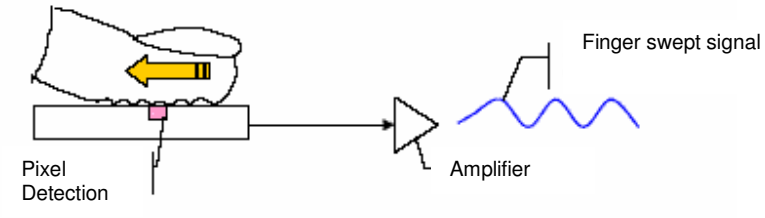
Images are sent slice per slice on host request.
Host first sets the FC109 in acquisition or navigation mode by sending a “set_mode” setup token to FC109 EP0. This initializes the analog array and selects the transfer size.
Host then sends setup tokens (slice-sized IRPs) followed by series of IN tokens to EP1 (EP2 in isochronous mode) and FC109 returns one data packet.
To stop transfer, host sends a new “set_mode” setup token on EP0 to return FC109 to idle mode.
After completion of a possible running FIFO access, FC109 will flush the FIFO and enter idle mode.
Slices transfers may be iterated until FC109 is returned to idle mode.

12. Wake Up (Refer to Wake up registers description)

The wake up mode is used to detect the first finger sweep on the sensor. The pixel array is switched off and only a specific pixel is used. The clock is supplied by an internal RC oscillator and dedicated to the very low consumption.

Functional Description
When the finger sweeps on the chip, ridge and valley series are detected. The signal is amplified and a state machine decides if the signal is compatible with a real fingerprint swipe. This method enables to automatically filter unwanted possible wake up events such as unintentional touches, and saves power as the host will not be wake up on such events.

Figure 12-1. Illustration of Finger Sweeping Sensor



Wakeup management
FC109 may wait finger swipe in a low power mode, or even wake the system by a user friendly finger sweep.
Host first sets the FC109 in low power mode by sending a standard setup token to FC109 EP0.
FC109 immediately stops any activity, enters idle mode, enables on-chip oscillator and waits for suspend signaling.
That is to say that host must stop sending “start of frame” tokens to FC109 USB segment.
After the USB legal inactivity delay, USB interface interrupts the MCU, which starts wakeup system, and “suspends” FC109, actually entering low power mode.
If a finger sweep is detected, remote wakeup request is returned to host through USB interface.
After detection of “start of frame” tokens, USB interface resumes from suspend mode and wakes MCU up.

13. Fake Finger detection

Fake finger detection

FC109 seamlessly monitors finger characteristics during acquisition.

Definition of fake fingerprints detection

Fake finger detection is based on skin electrical properties.
Two external conductive electrodes act as sensing device.

14. Memory bridge management

Serial interface

FC109 may serve as a bridge between host system and non volatile memory (EEPROM or flash). This memory may hold data, such as fingerprint templates, or useful non volatile information such as serial number, credentials, user preferences and so on.
Standard SPI memories are supported. After host has selected BRIDGE mode, transfer requests through EP0 are handled by the MCU in order to convey data between memory and USB. Serial memories differ with requests coding (write, erase, read, page selection …) and addressing length. In order to use any type of memory, protocol will be managed at application/driver level. FC109 will implement only a transparent mode.
SPI interface is configurable by software register access in phase and polarity to enable all kinds of SPI memory devices.
FC109 converts USB data packets into serial data flows and conversely.

The SPI has four modes of operation, 0 through 3. These modes essentially control the way data is clocked in or out of an SPI device. The configuration is done by two bits in the SPI control register (POL and PHA). The clock polarity is specified by the POL control bit, which selects an active high or active low clock. The clock phase (PHA) control bit selects one of the two fundamentally different transfer formats. To ensure a proper communication between master and slave both devices have to run in the same mode. This can require a reconfiguration of the master to match the requirements of different peripheral slaves.
The settings of POL and PHA specify the different SPI modes, shown in Table 14.1. Because this is no standard and specified different in other literature, the configuration of the SPI has to be done carefully.

Table 14-1. SPI Mode Configuration

SPI Mode	POL	PHA	Shift SCK-edge	Capture SCK-edge
0	0	0	Falling	Rising
1	0	1	Rising	Falling
2	1	0	Rising	Falling
3	1	1	Falling	Rising

The clock polarity has no significant effect on the transfer format. Switching this bit causes the clock signal to be inverted (active high becomes active low and idle low becomes idle high).

SPI transfer example

Read 4 bytes from an AT25F2048 memory.

- Configure SPI : FCTRL <= 30h
  (Custom instruction, value 03h, Index 0130h, Count 00h)
- Set SPI mode
  (Custom instruction, value 20h, Index 0003h, Count 00h)
- Configure transfer :
  (Custom instruction, value 0Ah, Index 0001h, Count 04h)
  4 bytes data = 03 (read instruction code) + 3 address bytes.
- Activate SCS : FCTRL <= 20h
  (Custom instruction, value 03h, Index 0120h, Count 00h)
- Start SPI transfer:
  (Custom instruction, value 08h, Index 0000h, Count 04h)
- Fetch SPI data : read EP0
- Reset SCS : FCTRL <= 30h
  (Custom instruction, value 03h, Index 0130h, Count 00h)
- Return to IDLE mode
  (Custom instruction, value 20h, Index 0000h, Count 00h)

15. Image quality management

If required, image quality may be increase by deferent ways:

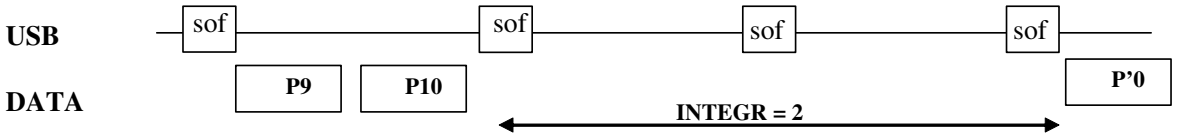
- ❖ Embedded contrast enhancement features.

The FC109 give the possibility to double the amplifier gain by setting the related control bit. Enhancement may be achieved without power consumption penalty.

- ❖ Relax Integration time.

Integration delay is defined by the number of USB frames between two image slices. Image blurring may occur if finger sweeping speed is too fast compared to acquisition speed. Actual delay may jitter by one USB frame, according to request instant of P10.

Figure 15-1. Integration time relaxing



- ❖ Optional PIX_TEST feature

Image contrast is proportional to the temperature difference between sensor and finger. According to the acquisition characteristics, image processing software may optionally trigger sensor temperature control through the PIX_TEST feature.

In order to limit current consumption when using the optional PIX_TEST feature, and in case of host failures, a watchdog is automatically triggered. Watchdog overflow stops module consumption after a 3 Seconds typical delay, based on USB frames timing. Contrast enhancement is automatically switched off in suspended or wakeup mode.

Owing to the power constraints of USB, the contrast enhancement function can be switched:

- OFF: contrast enhancement is not activated
- ON: contrast enhancement is activated

16. Power management

FC109 automatically switch off unused features to reach minimum power consumption.

17. Function Registers

17.1. Communication Interface Registers

Next list gathers register used for communication interface management.
Custom vendor commands are decoded by MCU and used to configure the FC109 device. Functional configuration is stored in the following registers.

Table 17-1. Communication Interface Registers

@	Rst	Access	Mnemonic	Description
0x00	0x00	RW	ACQ_CTRL	Acquisition Control Register
0x01	0x00	RW	FC109_CTRL	FC109 Features Control Register
0x02	0x00	R	STATUS	Status Register
0x03	0x00	RW	Threshold_WU	Wake up Threshold register
0x04	0x00	RW	Time_ WU	Wake up timings register
0x05	0x00	RW	Reserved 1	Write to 0
0x06	0x00	RW	Reserved 2	Write to 0
0x07	0x00	RW	Reserved 3	Write to 0
0x08	undef	RW	GPRH	General purpose register (msb)
0x09	undef	RW	GPRL	General purpose register (lsb)

Table 17-2. Versions structure

Offset	Rst	Access	Mnemonic	Description
0x00	0x00	R	REV_NUM	Device version (MAJOR / minor)
0x01	0x00	R	USB_VER	Firmware version (MAJOR / minor)

18.2 Registers Description

Table 17-2. Acquisition Control Register (ACTRL @ offset 00h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	GAIN	INTEGR.	INTEGR.	RESERVED	RESERVED	PIX_TEST_CTRL	PIX_TEST_CTRL	NOISE
Type	RW	RW	RW	-	-	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7	GAIN	Image gain Control: 0: 1x standard 1: 0.5x (reduced gain)
6:5	INTEGRATION	Set integration time. Delay acquisition by “integration” USB frames.
4	RESERVED	Always write to 0
3	RESERVED	Always write to 0
2:1	PIX_TEST_CTRL	PIX_TEST management. See notes below for details.
0	NOISE_REDUCTION	Initial pixel reset enable (active low) : when on, permanent pixel reset (RST_PERM) is forced to ‘1’ during the first 80th pixels of the first slice : 0 : On 1 : Off

NOTE: PIX registers can be used on this mode

PIX_TEST_CTRL		Description
0	0	OFF
0	1	Reserved
1	0	PIX_TEST: 30 mA consomption mode
1	1	Reserved

Table 17-3. Features Control Register (FCTRL @ offset 01h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	POL	PHA	DORD	CSVAL	Reserved	RFU	RFU	WU_CLR
Type	RW	RW	RW	RW	RW	R	R	RW
Reset	0	0	0	1	0	0	0	0

Bit	Mnemonic	Description
7	POL	Standard SPI clock polarity
6	PHA	Standard SPI clock phase
5	DORD	Standard SPI bit ordering: 0: MSB first (Usually used in SPI transfer) 1: lsb first
4	CSVAL	SPI Chip Select (active high by default) / GPIO value (led control for instance)
3	Reserved	Reserved
2:1	RFU	Reserved for future use
0	WU_CLR	Clear remote wakeup status bit (when written to ‘1’)

Table 17-4. Status Register (CTRL @ offset 02h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RFU				PIX_TEST_STAT	Reserved	WU_EN	WU_STAT
Type	R				R	R	R	R
Reset	0000				0	0	0	0

Bit	Mnemonic	Description
7:6	USB mode	00: not configured, 01: bulk, 10: full rate isochronous, 11: 1/2 rate isochronous
5:4	MODE	00 : idle, 01 : acquisition, 10 : navigation, 11 : memory bridge
3	PIX_TEST_STAT	PIX_TEST STATUS: 0: Off 1: On
2	Reserved	Reserved
1	WakeUpEn	Status of USB feature “remote wakeup”: 0: Off 1: On
0	WakeUpStat	Remote wakeup status (cleared by WU_CLR) : 0 : none 1 : latest exit from USB suspend was from remote wakeup.

Table 17-5. Threshold Wake Up Register (Threshold_WU @ offset 03h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	-	-		-		WU_EVENT_TH		
Type	R	RW		RW		RW		
Reset	0	0x0		0x0		0x0		

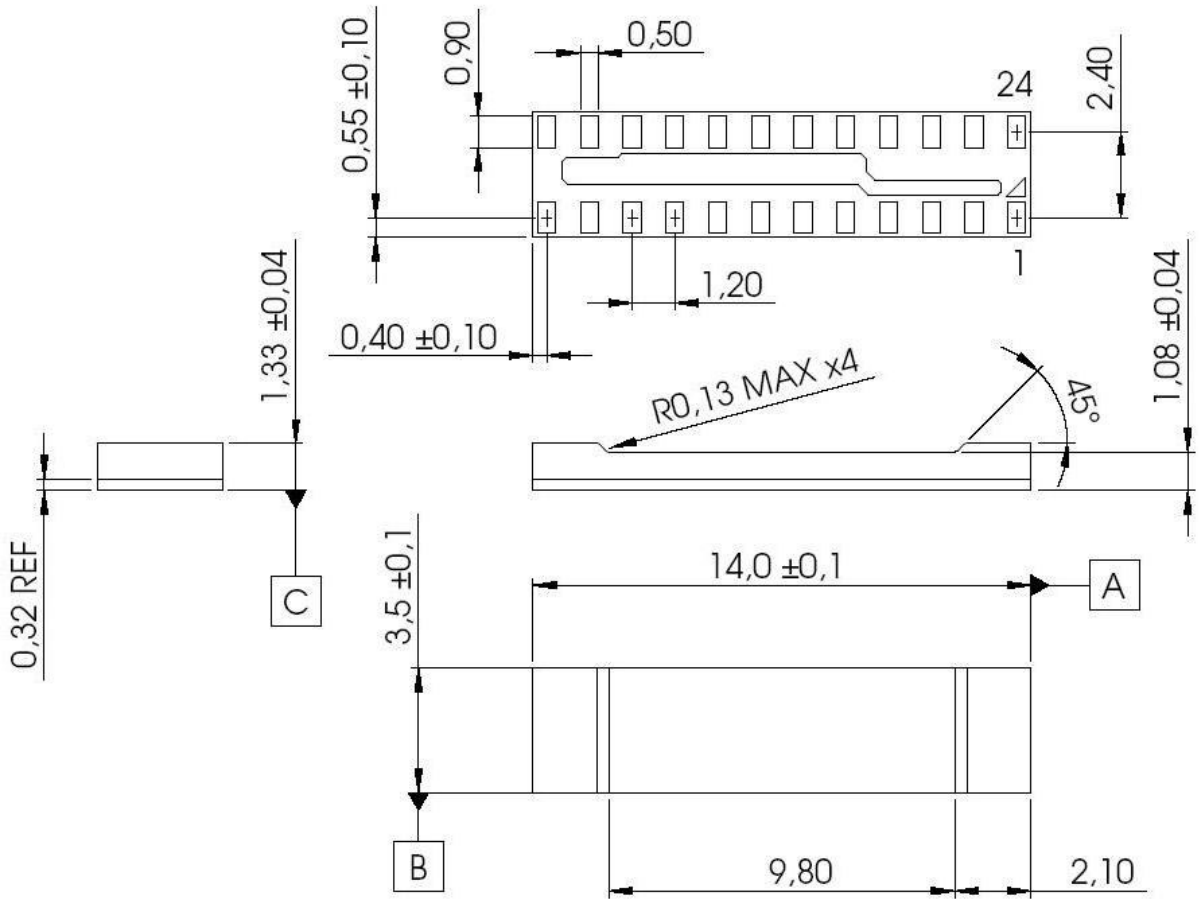
Table 17-6. Time Wake up Register (Time_WU @ offset 04h)

Bit	7	6	5	4	3	2	1	0
Mnemonic	RFU	RFU				WU_TI	-	
Type	R	R				RW	RW	
Reset	0	0x0				0x0	0x0	

Notes: 1.Typical values are: 02h in 0x03 register and 04h in 0x04 register for a fast wake up
06h in 0x03 register and 04h in 0x04 register for a slower wake up

17.1.1.1.1. Packaging Mechanical Data

Figure 18-1. AT77C109A- ZD01YV Package Information



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: X.XX ± 0.08 ANGULAR: ± 1°	ANGLE OF PROJECTION DO NOT SCALE DRAWING

18. Ordering Information

Figure 19-1. Package device

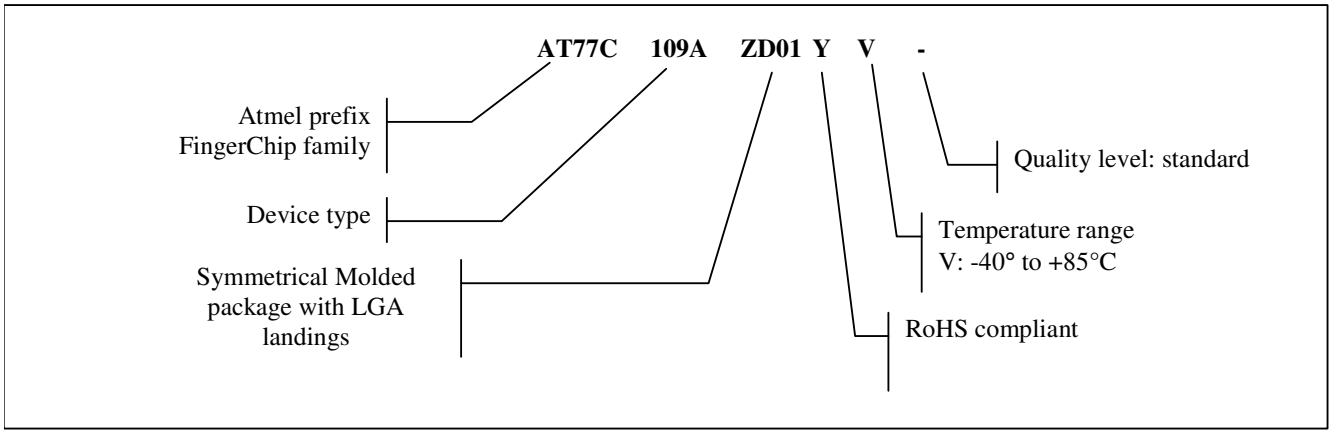


Table 4-5. Package information

Part Number	Package	Operating range	Comments
AT77C109A-ZD01YV	24-pin Molded	–40C to +85C	Without Electrodes

Revision History

Table 20-1. Revision History

Doc. Rev.	Date	Comments
A	04/28/2008	Initial document release.

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