THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

FingerChip™ Family

PRELIMINARY SPECIFICATION

FC8X8
500 dpi 0.315" x 0.315" fingerprint sensor

1. DESCRIPTION

FC8X8 is part of the FingerChip™ TCS monolithic fingerprint sensor family.

FC8X8 is a single chip, high performance, low cost sensor based on both pressure and temperature physical effects for fingerprint sensing.

Thanks to the combination of those two effects, FC8X8 gives to fingerprint recognition systems an efficient way to solve the "dead or alive" dilemma.

The sensitive layer is deposited over a CMOS image device, enabling output of an accurate fingerprint image.

The present product has a160x160 pixel array, with a pixel pitch of 50 µm (500 dpi). Sensor area is 8 mm X 8 mm (0.315" X 0.315"), allowing the capture of a fingerprint image.

In nominal operation, the device delivers images at a rate of 36.8 images per second.

Demonstration board is available under reference FCDEMO1.

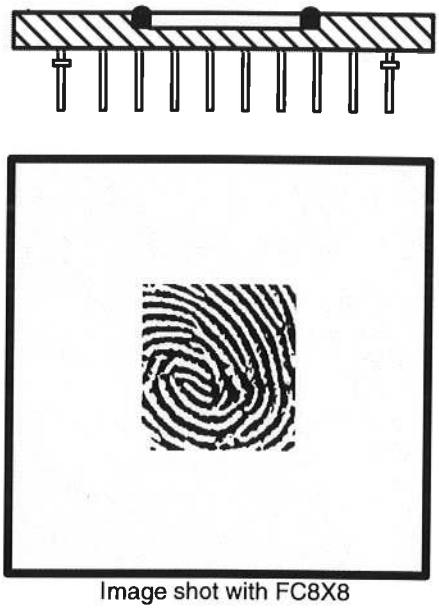


Image shot with FC8X8

2. MAIN FEATURES

- MONOLITHIC low volume flat sensor
- Sensitive layer associated to a CMOS array insuring live fingerprint capture (1.2 µm CMOS technology Double Level Metal)
- Heat and pressure of the finger detected: living finger.
- No optics, no prism, no light required.
- Image zone : 8 x 8 mm = 0.315" X 0.315".
- Array: 160 x 160 pixels.
- Pixel pitch : 50 µm x 50 µm = 500 dpi.
- Power consumption : 280 mW @ 5v, pixel clk = 1MHz, 25°C.
- Sampling in Ceramic package CPGA68.
- External pixel clock : 1MHz
  Internal line clock : 5.88 kHz
  Internal Frame clock : 36.8 Hz

3. APPLICATIONS

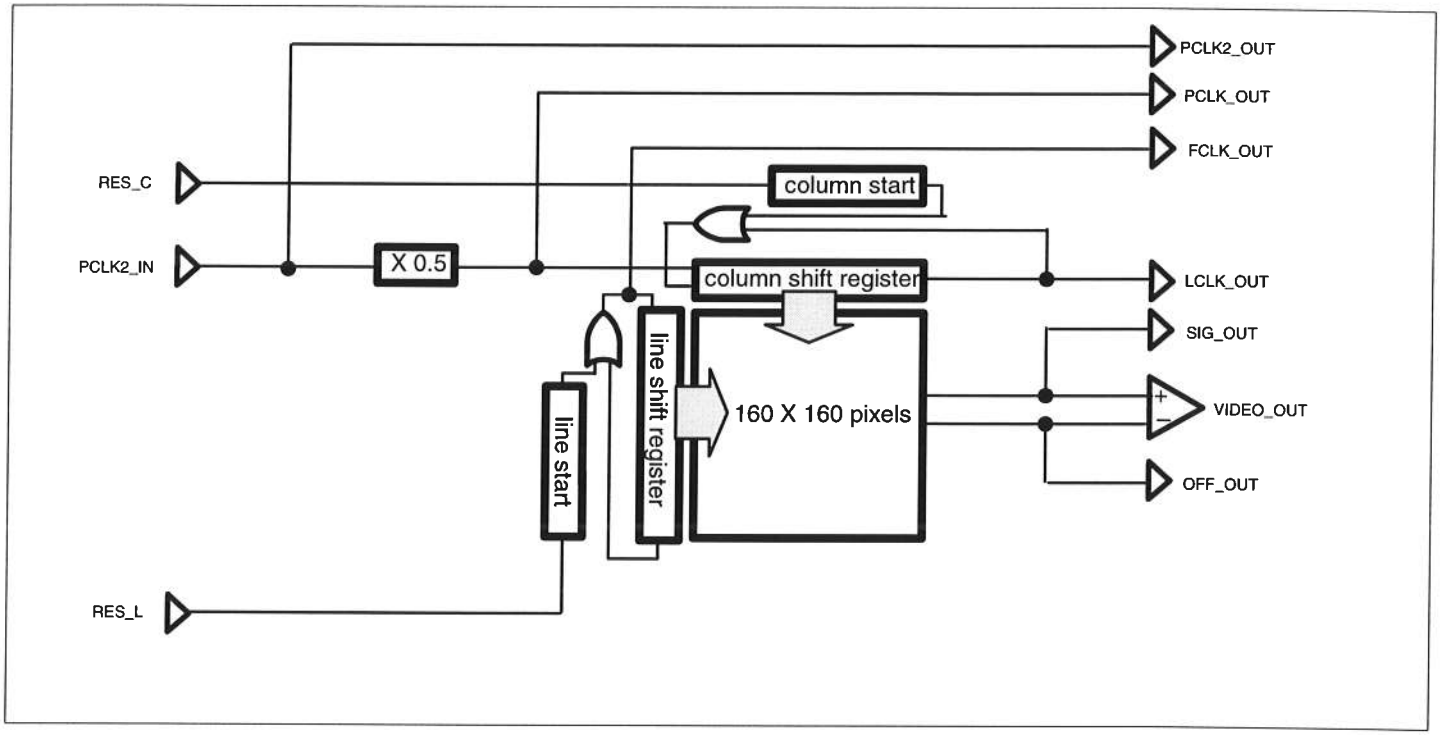
All devices that requires authentic acceptance, especially portable devices.

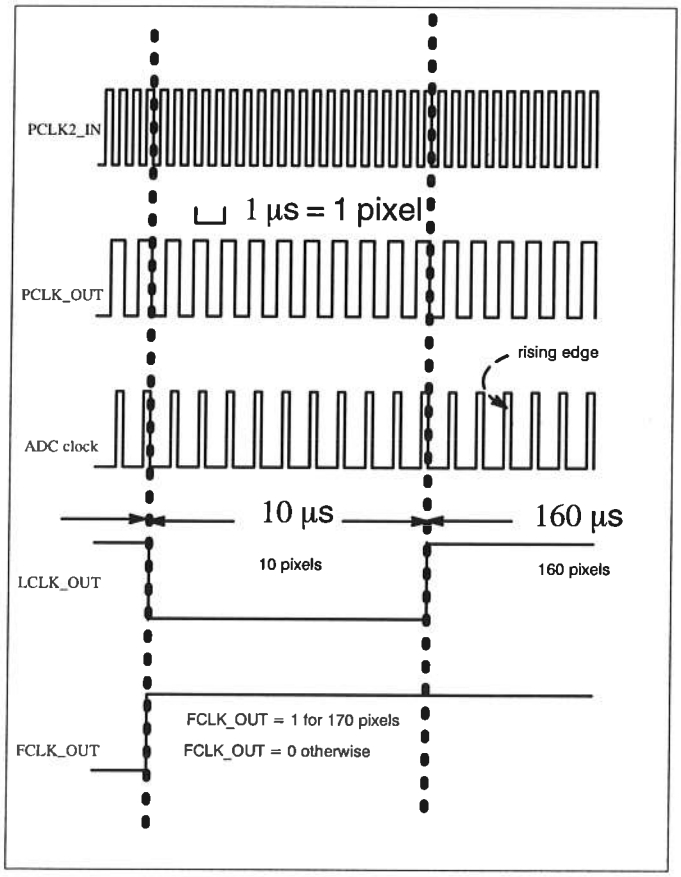
- Terminal Access (Multimedia PCs, access to networks, etc...)
- Electronic payment associated with smart card (ATM –Automated Teller Machine–, Portable POS –Point Of Sale–, etc...)
- Building access
- Electronic keys (cars, home, ...)
- Cellular phones (usable only by registered users)
- Weapons (usable only by registered users)
- Portable fingerprint recorders for law enforcement
- ...

4. PIN IDENTIFICATION

FPL	D2	front plane	0v
GND_LOG	D1	logic ground	0v
VDD_LOG	C3	logic power supply	5v
RES_C	C2	column shift register reset	TTL active high
VDD_ANA	C1	analogic power supply	5v
GND_ANA	B1	analogic ground	0v
GND_BUF1	B2	buffer ground	0v
VDD_BUF1	B4	buffer power supply	5v
FCLK_OUT	A2	frame clock output	TTL 36.76 Hz
VDD_AOP	A3	output amplifier power supply	5v
SIG_OUT	A4	positive input of amplifier	4v – 5v
VIDEO_OUT	B5	video output	1v – 3v
REF_IN	A5	reference voltage of amplifier	1.2 – 1.8 v **mandatory**
POLAR	A6	amplifier poling	1.1v **internal value**
OFF_OUT	B6	negative input of amplifier	4v – 5v
VDD_BUF2	A8	buffer power supply	5 v
GND_BUF2	A9	buffer ground	0 v
GND_PIX	B7	pixel ground	0 v
PCLK_OUT	A10	pixel clock output	TTL 1 MHz
PCLK2_OUT	B9	double pixel clock output	TTL 2 MHz
PCLK2_IN	B10	double pixel clock input	TTL 2 MHz
ENSP_IN	C10	clock enable	not used 0v
RES_L	C9	line shift register reset	TTL active high
GND_PROT	C8	ground protection	0 v
LCLK_OUT	D10	line clock output	TTL 5,882 kHz
VDR	D9	pixel reset voltage	1.13 v **internal value**
	A1	seal ring	0 v
	E2	die attach	0 v

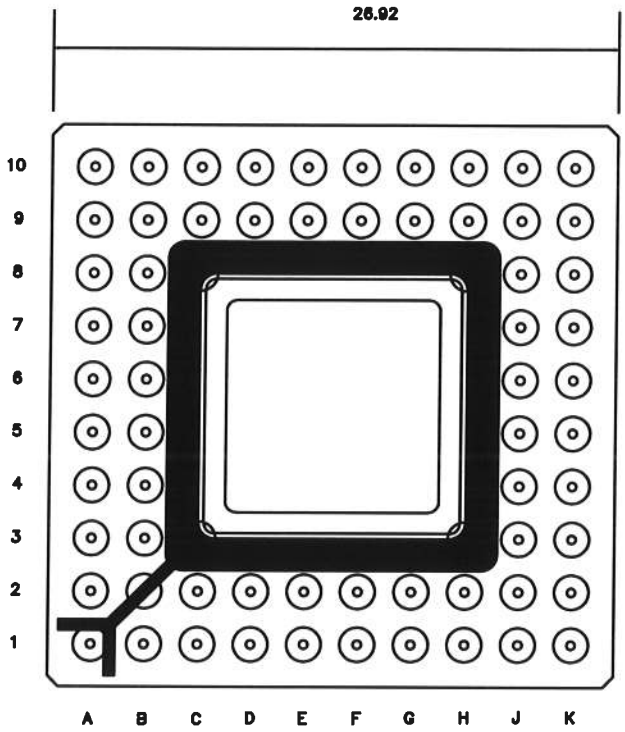
5. BLOCK DIAGRAM and CHRONOGRAM

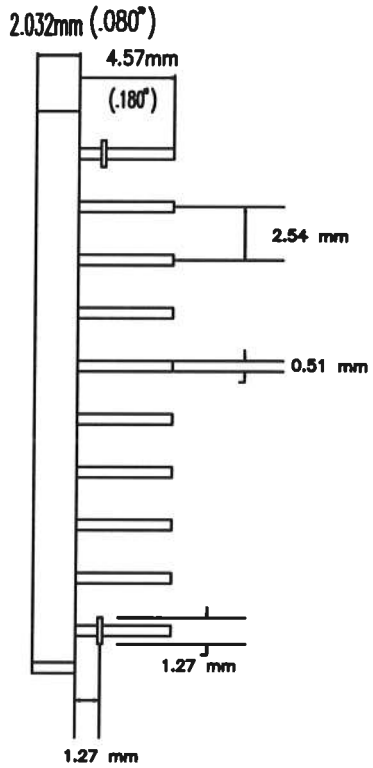




- PCLK2_IN is the external clock at a rate of 2 MHz.
- PCLK2_OUT is the output of the external clock at a rate of 2 MHz.
- PCLK_OUT is the pixel clock output at a rate of 1 MHz. A pixel is read during 1 µs.
- An ADC can be added to digitize the VIDEO_OUT signal at a rate of 1 MHz. The output amplifier can drive an impedance of 3 kΩ, 5 pF. The ADC sample clock is obtained with a AND operation on the PCLK_OUT and PCLK2_OUT signals. The rising edge is used to trigger the ADC. The dynamic range of the ADC should be set between 1 and 3 volts.
- RES_C is the column shift register reset, which is active on high level. When released, the first column is selected.
- RES_L is the line shift register reset, which is active on high level. When released, the first line is selected.
- LCLK_OUT is the line clock output. It is set to low level during 10 µs. This time is the interval between two lines. The same interval is used between the last and the first line. When a line is selected for reading and reseting, LCLK_OUT is set to high level, during 160 µs.
- FLCK_OUT is the frame clock output. This output is set to high level during 170 µs when the first line is selected.

6. CERAMIC PACKAGING





This product is manufactured and commercialized by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - PO Box 123 - 38521 SAINT-EGREVE Cedex - FRANCE.

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